DESIGN OF LOW POWER DYNAMIC COMPARATOR WITH REDUCED KICKBACK NOISE USING CLOCKED PMOS TECHNIQUE

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ABSTRACT

The Dynamic comparator is a basic building block of all analog to digital converter architectures. The need for low power dynamic comparators is essential to maximize speed and power efficiency of the ADC architectures. Normally, dynamic latched comparators suffer from kick back noise effect. A novel dynamic latched comparators with clocked PMOS technique is proposed in this paper. Simulation shows that the power consumption and kickback noise effect of the proposed dynamic comparator is 952.4µW and 1.1mVwhich is very less when compared with the conventional dynamic comparators The area occupied by the proposed comparator is 0.00218mm^2. The simulated kick back noise effect of the proposed dynamic latched comparator is about 80% less than the conventional dynamic latched comparator with 1.8V supply.

Keywords: Dynamic latched comparator, Kickback noise, Clocked PMOS Technique, Low Power

1.INTRODUCTION

Comparator is one of the basic building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area[1]. Therefore, the characteristics of comparators determine the performance of ADCs. The trend of achieving both higher speed and lower power consumption in these applications makes dynamic latch comparators very attractive, as they achieve fast decisions by strong positive feedback [2] and no static power consumption. However, comparator suffers from the disturbance of the input signal source due to kickback noise and DC static off-set. In static latched comparator the injected current through the coupled parasitic capacitor produces a kickback noise over the input impedance. This kickback noise can disturb the input signal and leads to errors [3].

Kick back noise is due to the back flow of the output signal to the input. This back flow occurs mainly due to the feedback

mechanism, which include both positive and negative feedback. The comparator suffers from the differential and common mode kickback noise effect. Common mode kick back noise occurs due to the switching of the source nodes, and the differential mode kick back noise occurs when there is a large variation in the voltage drop across the output nodes when the clock is low.

In addition to the differential kickback noise caused by the outputs of the comparator, the clocked input generates also the common mode kickback noise. Especially when the signal source has asymmetric impedance, the common mode kickback noise becomes even worse[4]. In ADCs [5,6], where the comparators are connected in parallel, the kickback noise can considerably disturb the input signal and limit the performance of ADCs.

In the reset phase of regenerative latched type comparator[7],both inverters are shorted by the switch. In the regeneration phase the switch opens and the positive feedback regenerates the outputs to supply rail voltages, respectively. But the large variation of output voltages is coupled by the gate-drain capacitance of the input transistors back to the input nodes. Thus, the injected current through the coupled parasitic capacitor produces a kickback noise over the input impedance. This kickback noise can disturb the input signal and leads to errors. Single stage dynamic comparators are widely adopted with the advantages of fast speed and zero static power consumption, but they combine the latch function with the input stage, which increases the number of cascading transistors from supply voltage to ground and limits the overdrive voltage of the input transistors[8]. As a result, it restricts the period of the input transistors operating in saturation region and degrades the comparator's noise performance.

In this paper a double tail comparator with clocked PMOS technique with low kickback noise for high speed and low power Pipelined ADCs is presented. The proposed Comparator architecture employs a clocked PMOS technique where the node voltage is pulled to VDD when the clock is low. This removes the uncertain voltage at the clocked PMOS node. Also the intermediate stage formed by the two transistors MR1,Mr2 passes the voltage Vfn(p) to the cross coupled inverters and it provides a better shielding between the input and the output the kick back noise is significantly reduced. Simulation results of the proposed comparator show a remarkable level of kickback noise reduction compared with conventional latched comparators.

2. REVIEW OF COMPARATOR ARCHITECTURES

A conventional double-tail comparator is shown in Fig.1 [9]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the

input stage (small Mtail1), for low offset. The operation of this comparator is as follows:[10] During reset phase (CLK = 0, Mtail1, andMtail2 are off), transistors M3-M4 pre-charge f_n and f_p nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes f_n and f_p start to drop with the rate defined by $IMtail1/C_{fn}(p)$ and on top of this, an input-dependent differential voltage $V_{fn}(p)$ will build up. The intermediate stage formed by MR1 and MR2 passes $V_{fn}(p)$ to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

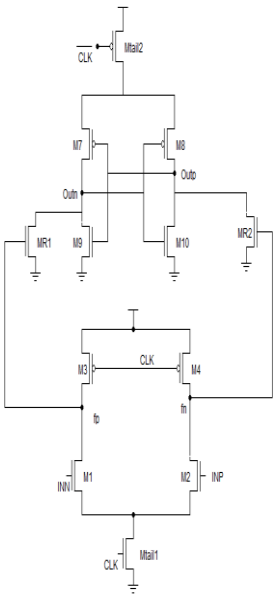

Fig.1 Conventional double tail comparator.

The typical dynamic latched comparator shown in Fig.2.It is the most power-efficient comparator, because it has no pole at the preamplifier stage and no static current. But it produces the highest kickback noise at the input. Not only the differential kickback noise but also the common-mode kickback noise is very high. This is caused by the large voltage shift of the D/S nodes of the input differential pair. In the reset phase, the drain nodes of the input pair are reset to VDD and the source nodes of input pair float also in high voltage level. Once the comparator is triggered into regeneration phase, the D/S nodes of input pair start falling together. This large variation of falling D/S nodes of input pair induces the common-mode kickback noise. Furthermore, this comparator has four transistors in stack. The characteristics of differential kickback noise have been optimized by dividing the input and the latch in two stages. In each stage only three transistors operate. However, the input pair still suffers from high common-

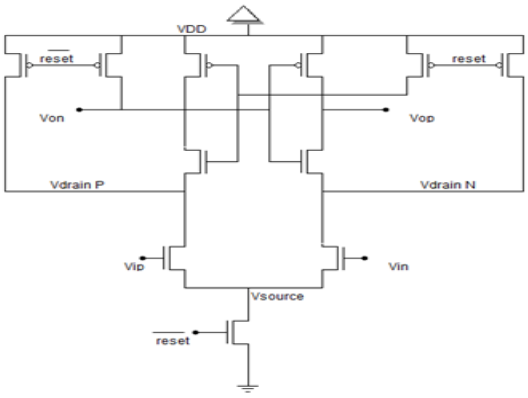

Fig.2 Dynamic Latch Comparator[12]

The Dynamic Comparator with reduced kickback noise is shown in Fig. 3.

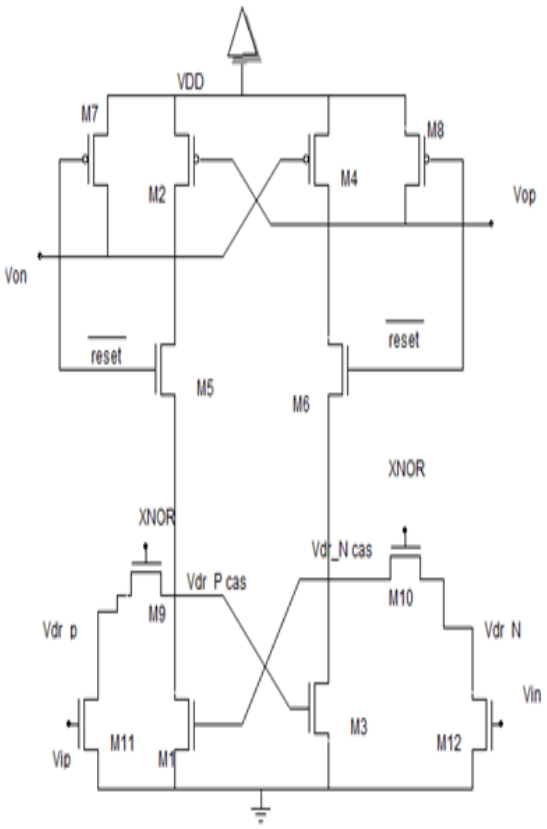

Fig.3 Dynamic Latched Comparator with reduced Kickback Noise[4]

The input pair is implemented by the common source pair M11/M12. Because the source nodes of the input pair are always connected to ground, generation of common-mode kickback noise by switching of the source nodes is prevented. The input common source transistors sink the current from the regenerative cross-coupled inverters M1/M2 and M4/M3. In the reset phase, where the reset is logic low, M7/M8 PMOS transistors are turned on, clamping VON and VOP to VDD. The switch transistors M9/M10 are also turned on by the XNOR gate, which is controlled by the output signal V_{on}/V_{op}. Once reset goes high for the regeneration phase, the NMOS transistors M5/M6 are turned on, whereas PMOS transistors M7/M8 are off. So the voltages of V_{on}/V_{op} start falling from VDD. Depending on the current drawn by the common source input pair M11/M12, the voltage difference between the falling voltages of V_{on}/V_{op} will be further enlarged by the regenerative cross-coupled pair, until the comparator outputs reach the supply rail voltages. [4]

3. PROPOSED DYNAMIC COMPARATOR

The key idea of the proposed comparator is to reduce the kickback noise and power. The operation of the proposed comparator is as follows in Fig.2. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

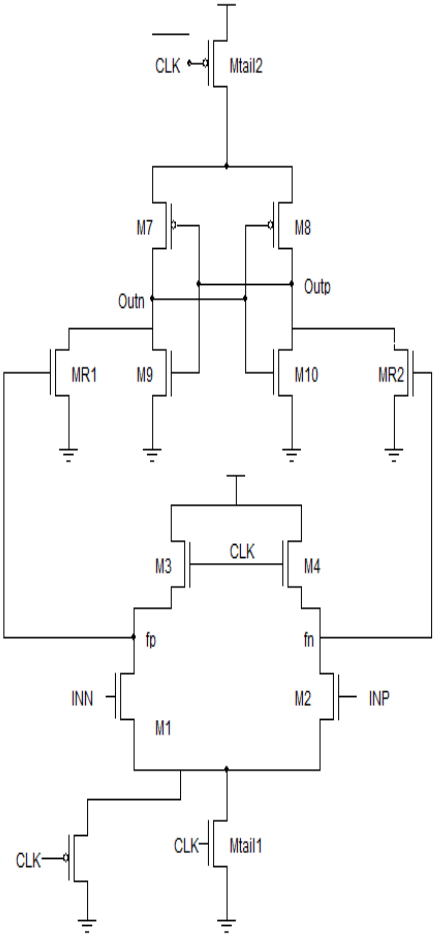

Fig. 4. Proposed dynamic comparator with reduced kickback noise.

Further the kick back noise can be reduced by using clocked PMOS transistor method. Here the clocked PMOS transistor is added to pull up the node voltage to VDD when CLK is low. This act removes the uncertain voltage at the clocked PMOS transistor node and thus the voltage of the sampling capacitor will not be drifted. The expense of this change is slightly slowing down the recovery time.

4. RESULTS AND DISCUSSION

The proposed comparator has been designed for 10-bit pipelined ADC.A kickback noise simulation has been implemented in designed ADCs, based on the 180nm CMOS technology. The supply voltage is 1.8 Volt.

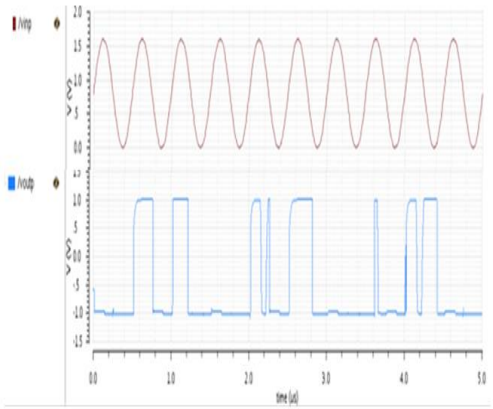

Fig.5 Transient Simulation of Double tail Dynamic Comparator

Fig.5 shows the transient simulation of double tail dynamic comparator. As it can be referred from the output wave form, the Dynamic comparator suffers from kickback noise. The glitches in the output wave form is due to the presence of kickback noise. The value for the kickback noise can be calculated from the graph and the value is 5.1mV. The input waveform is compared with the reference voltage, which is 0.45V. If the voltage of the input is less than the reference voltage, then the output signal goes high, and when the input signal goes low, the output goes low.

The kickback noise is reduced by Clocked PMOS transistor technique. Addition of the Clocked PMOS transistor at the input node will pull up the voltage at that node, which reduces the kick back noise effect which is

caused by the large variation in the voltage drop across the node. With the introduction of clocked PMOS technique the kick back noise in the comparator is reduced from 5.1mV to 1.1mV.

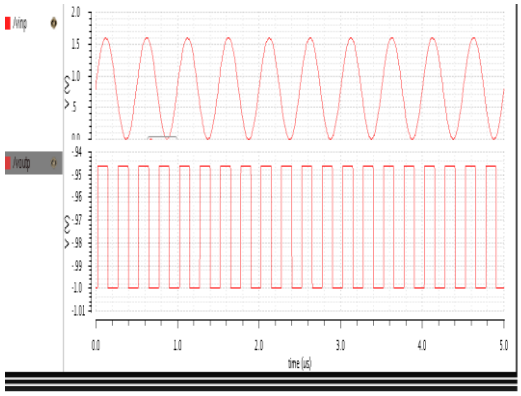

Fig.6 Transient Simulation of proposed Double tail Dynamic Comparator

Fig.6 &7 shows the transient simulation of proposed double tail dynamic comparator. As it can be referred from the output wave forms, the kick back noise in the conventional double tail comparator is significantly reduced.

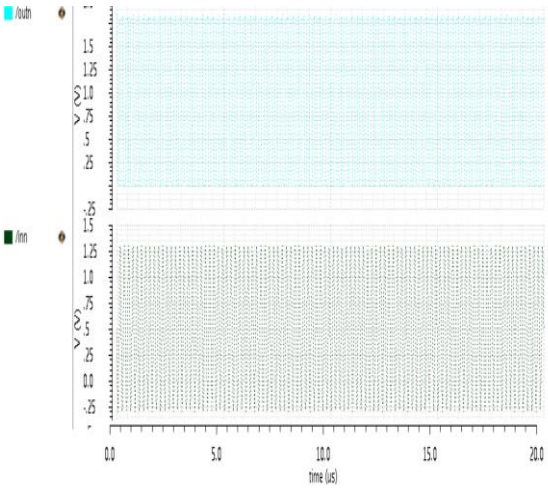

Fig.7 Transient Simulation of proposed Double tail Dynamic Comparator @fin=1GHz.

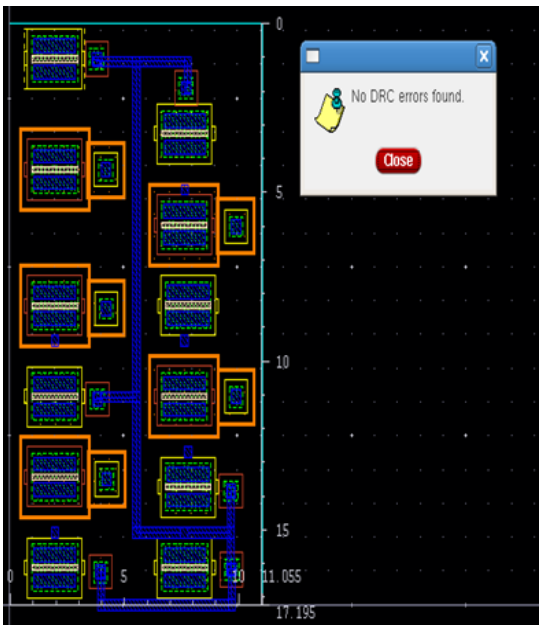

Fig.8 Layout of Conventional double tail dynamic comparator

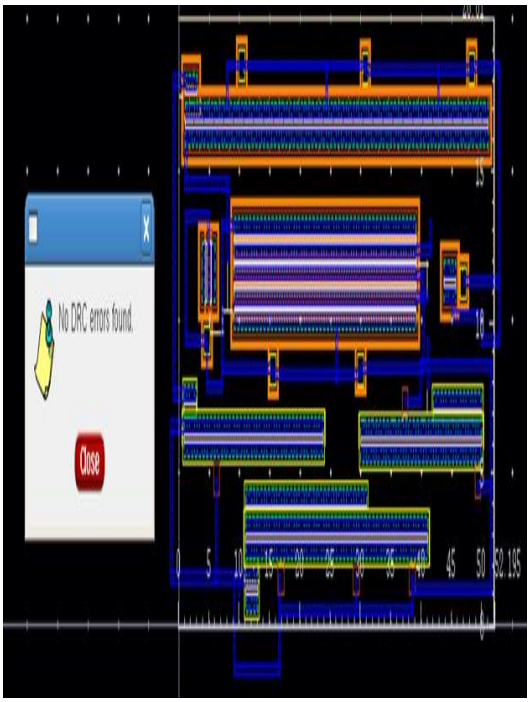

Fig.9 Layout of Dynamic latch Comparator

Fig.8shows the layout of conventional Double tail Comparator. The obtained area is 00019009mm^{2}. Fig.9 shows the layout of the Dynamic Latch Comparator. The obtained

area is 0.001042 mm^2.Fig.10 shows the layout of the proposed Dynamic Comparator. The obtained area is 0.0002184mm^2.

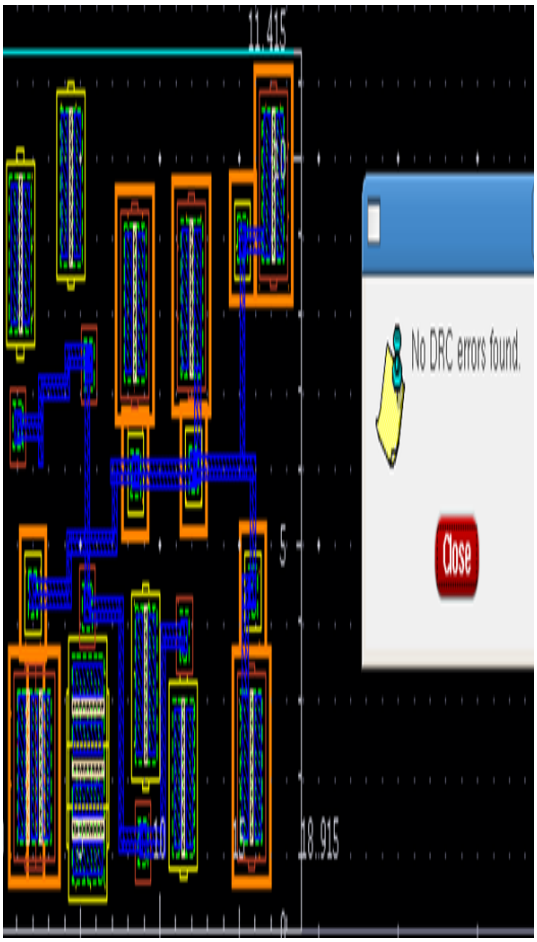

Fig.10 Layout of Proposed double tail Dynamic Comparator

Simulation results show that the proposed double tail dynamic comparator consumes 952.4µW which is very less than the conventional dynamic comparator. Even though there is 9.52% increase in the area occupied the power consumption of the proposed dynamic comparator is reduced significantly. In the proposed comparator about 66% of power reduction has been achieved. After the introduction of clocked PMOS transistor technique, the kickback noise is reduced from 5.3mV to 1.1 mV when compared with the conventional dynamic comparator. Hence the proposed double tail dynamic comparator is suitable for high speed and low power pipelined ADCs.

Table1. Performance Summary of Proposed Double tail Dynamic Comparator.

Parameters	**Values**
Technology	180nm
Supply Voltage	1.8V
Input Frequency	1 GHz
Power Consumption	885µW
Kick back noise Voltage	1.1mV
Offset Voltage	0.5V
Delay	430ps
Area	0.0002184mm^2

Table 1 shows the Performance summary of the proposed Double tail dynamic comparator. Table 2 shows the Performance comparison of the simulated comparators including the Dynamic latch ,Conventional and proposed double tail dynamic comparator. The offset voltage is 0.5V and the delay obtained is 450ps. When the supply voltage is changed from 1V the delay is 24ns,for 1.2V the delay is 24.47ns,for 1.4V the delay is 420ps and for 1.6V the delay is 425ps and for 1.8V the delay obtained is 430ps.

Table 2 Performance comparison of proposed comparator with other types of dynamic comparator

Types of Comparator	Kickback noise(mV)	Obtained Power(mW)	Area($mm^{2)}$
Dynamic Latch Comparator	3.778	3.7	0.001042
Double Tail Comparator	5.1	2.684	0.0001900
Proposed Comparator	1.1	885.5	0.0002184

Table 3. Comparison of proposed comparator with other reported comparators.

Ref.	Technology(nm)	Supply Voltage(V)	Comparator	Power Consumption (µW)	Kick back noise (mV)	Area(mm^2)
[1]	180	1.2	Double-Tail	1400	5.3	0.000392
[13]	180	1.8	Dynamic	900	-	-
This work	180	1.8	Double –Tail with PMOS Technique	885.5	1.1	0.0002184

The performance of proposed comparator is compared with other reported comparators in Table3. The proposed technique is comparatively a good option, because, with the addition of the clocked PMOS transistor at the common source input transistor pair, the voltage is clamped back to the Vdd. This will reduce the common mode kick back noise, which is occurring due to the large voltage variation. Since with the addition of the clocked PMOS transistor, the occurrence of the large voltage variation will not take place, thus reducing the kickback noise in the circuit. Addition of additional transistor, one of the kickback noise reduction technique, is implemented [1], but with the clocked PMOS technique only the kickback noise was considerably reduced.

CONCLUSION

With the development of the technology, the integrated circuit becomes smaller and smaller, which means low power circuit is demanded recently. The need for low power dynamic comparators is essential to maximize speed and power efficiency of the ADC architectures. Low power dynamic comparator with reduced kick back noise is designed with a power consumption of 952.4μW at 2MHz and an area of 0.0002184mm^2 in 180nm CMOS process by using CADENCE Software.

ACKNOWLEDGEMENT

The authors are grateful to the management of Karunya University and VLSI Centre of Excellence of the School of Electrical Sciences, ECE Department, Karunya University for facilitating this research work.

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