PRACTICAL SET UP TO TEST A NOVEL NEUTRAL POINT OSCILLATION MITIGATION TECHNIQUE FOR THREE LEVEL INVERTER

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Abstract: *A perceived and existing issue with three phase neutral point clamped (NPC) inverter is the unbalancing voltage at the neutral point. This is due to various factors like manufacturing tolerances of capacitors, difference in switching times, uneven discharging and charging of capacitors, effects of motoring and regenerative operation. Due to neutral point voltage deviation the output voltage gets distorted and low power harmonics also appear. The neutral point stabilization is done by various methods like carrier-based PWM, space vector PWM, hybrid PWM, selective harmonic elimination. The conventional carrier based PWM technique doesn't provide a valid solution for all power factors and SVPWM is complex in implementation and increases switching losses, In this paper a novel carrier-based PWM technique is proposed in which level shifting of carrier wave is done based on neutral point voltage and current feedback. This is implemented in MATLAB/SIMULINK and a Hardware setup is developed with DSP controller.*

Key words: *CB pulse width modulation, NPC inverter, Dc link instabilization, DSP controller, CCS, Neutral point stabilization.*

1. Introduction

The multilevel converters era has been started in 1975 and are used in high power medium voltage Industrial applications [1]. Multilevel inverter is to synthesize a near voltage from several levels of dc voltages. As number of levels increases, the synthesized output waveform has more steps that approaches a desired waveform. The steps are added to waveform, the harmonic distortion of the output wave decreases. To obtain a quality output voltage or current waveform it is required to switch the inverter with high- frequencies using various PWM strategies [2]. The increased switching frequency increases the stress on the switch. But for a multilevel inverter with same power level as each switch has to carry only one level of voltage switching stress decreases. The multilevel inverter has been used in different applications like traction drive system, VAR compensation and enhancement active filtering, high voltage motor drive, high voltage dc transmission, FACTS [3]. Multilevel inverters are classified into Diode clamped multilevel inverter, Flying - capacitor multilevel inverter, Cascaded multilevel inverter. The major problem with three level inverter is neutral point instabilization. Due to neutral point deviation the distorted voltage occurs the load and low frequency neutral point oscillations also occurs. For balancing neutral point voltage different schemes are proposed in literature they are: Carrier base PWM, Space vector PWM, Selective harmonic elimination modulation [4]. The existing technique to neutralize the neutral point voltage oscillation is the OFFSET "f" of appropriate polarity is added to reference wave results in DC bias in the neutral current that serves the neutral point voltage [5]. Another one is in the space vector PWM the redundant states are used to control neutral point oscillation. The drawback of this is complexity of control logic for Neutral point stabilization and output waveforms [6].

In this paper, a new of Carrier Base PWM scheme is presented to overcome the existing technique drawbacks. The modulator is tested by using Matlab/Simulink and developed by using DSP controller. For these Simulation and Experimental results are presented and conclusions are drawn.

2. Diode Clamped Multilevel Inverter

Three-level Neutral point clamped (NPC) Inverter is the most well-known topology of multi-level conversion systems. Figure.1 shows the NPC

inverter circuit diagram. The common three level inverters are noteworthy for high power applications. It was invented first by Nabae in 1981 [7]. The main drawback of this model is capacitors unbalancing or neutral point instabilization. In a three level inverter, an array of 4 switches and 6 diodes make the leg of NPC to be switched to Vdc/2, 0, -Vdc/2. The main advantage of this inverter is diodes will allow only a little amount of voltage, so finally stress on each electrical device is reduced. To balance the capacitor voltage unbalance and to rectify Neutral point instabilization a Novel level shifted carrier base PWM with closed loop system is implemented.

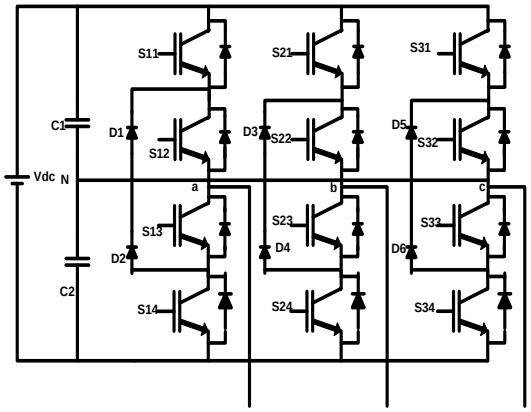

Fig.1: Three phase NPC inverter

3. Proposed Technique

The proposed technique "A Novel Level Shifted Carrier Base PWM with Closed Loop System" is opted for three level Diode Clamped Multilevel inverter. Whenever the inverter is triggered Charging and Dis-charging modes of capacitors occurs and creates uneven voltage distribution between switches which may leads to Neutral Point Instabilization, to stabilize the neutral point, proposed technique has been developed.

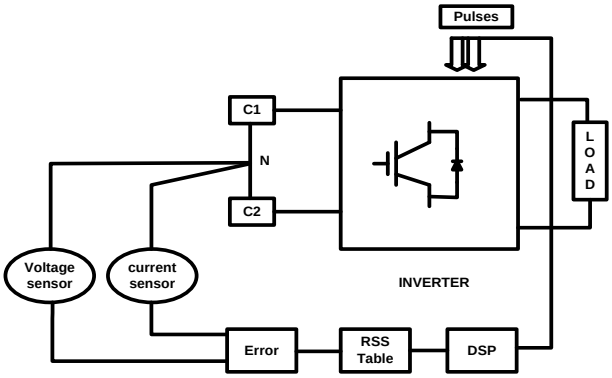

Figure.2: Block diagram for proposed technique

The proposed technique works as, voltage sensors and current sensors are placed across capacitors and neutral point. After triggering the inverter the difference voltage (Vc1-Vc2) and Neutral current are sensed by sensors. From the Table.1 it can be observed that the voltage difference and neutral current signs are obtained, after knowing signs the Error (e) decides the shifting of the carrier signal to positive side or negative side of the DC bias. RSS table is used to set the level shift of the carrier signal which is compared with reference signal. The objective of the RSS table and level shifted PWM generation is shown in figure.3. Due to the charging and discharging nature of capacitors the voltage difference or error is appeared, this error voltage magnitude chooses the dc offset to be added or subtracted to the carrier signal using RSS Truth table. By this the ON-OFF time periods of switches are managed, that means ON time period of the switch is maintained more time than OFF time switch or OFF time of the switch maintained more time than ON time switch or vice-versa with this Duty Ratio also changes, overall the Pulse width increases or decreases that serves to balance the neutral point balance.

Sign(V_{c1}-V_{c2})	**Sign(I_n)**	**Error(e)**
0	-	0
1	1	-1
1	-1	1
-1	1	1
-1	-1	-1

Table 1: RSS Truth table to increment or decrement the Value of e for neutral-point voltage balancing

IV. Simulation model of proposed Concept

The performance of three-phase neutral point clamped inverter is Simulated in the Matlab/Simulink by choosing the input as Vs=400v, R, L Load=50 ohm and 1mH, Capacitors C1=C2=10mf.

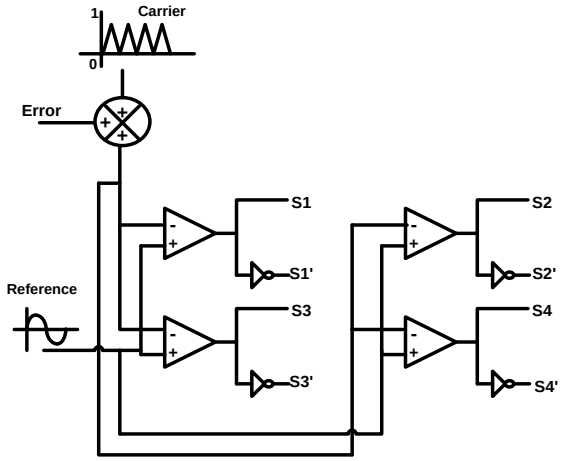

Fig.3. proposed control technique for simulation

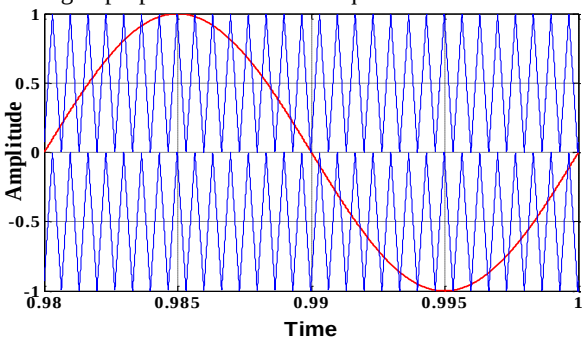

Fig.4. Sine PWM comparison

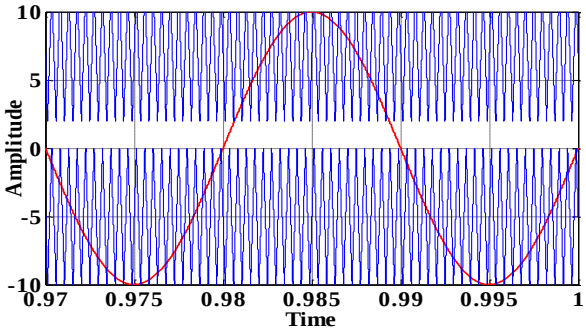

Fig.5. Level shifted comparison

Figure 4 and Figure 5, shows the comparison of carrier and reference signal of conventional SPWM and proposed technique with fundamental frequency 50Hz, the modulation index is 0.8 and device switching Frequency is 1000 Hz using figure.3 model.

5. Hardware description

In practical open loop neutral point clamped inverter is developed with 3KW load in the laboratory. This set up involves development of, printed circuit board (PCB) designed Buffer circuit, PCB designed Gate driver circuit, Transformer, Three phase MOSFET switches circuit, Capacitor bank, Regulated power supply (RPS).. For triggering the inverter Sine PWM pules with level shifted carrier base are generated using DSP TMS320F28335 control board. The description of circuits, equipment used in hardware development is discussed below.

Buffer circuit:

DSP generated signals are not sufficient to drag the current. So to amplify the current of DSP buffer circuit is connected that gives sufficient current turn on IGBTs. Fig.6 is buffer circuit designed to amplify current from DSP output signals. Buffers are driving chips, that they boost some characteristics of the circuit. In this case, the current is increased without compromising voltage. Buffer is used to boost the current so that each device may operate properly. A typical gate supplies approximately 1mA- if buffer is added this may upto 15mA.

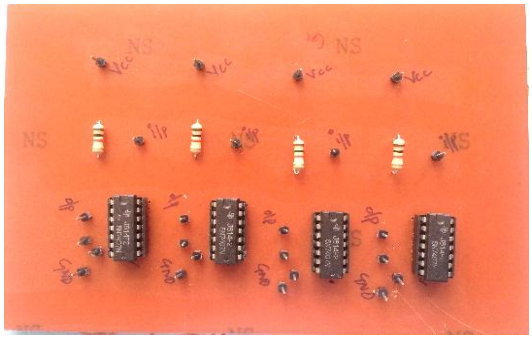

Figure.6. PCB designed Buffer circuit

Gate Driver Circuit:

Gate driver circuit provides both positive and negative voltage for MOSFETs that is to turn ON switch positive voltage and turn off switch negative voltages are given. So, gate driver is known as bipolar voltage supplier. Gate driver is used for Electric Isolation between Control and Power circuit. Primary elements of isolation and gate driver circuit are – To give required gate voltage and current to MOSFETs for switching, To transmit the control signals to the bridge circuit faithfully, Provides electrical isolation between power switch and control circuit. Driver

circuit amplifies control signal to required level for switching of power switch. The TLP250 driver has an output stage and a power supply connection. The extraordinary thing about the TLP250 is an optically isolated driver, meaning that the input and output are optically isolated. Figure.7 shows the circuit board of gate driver used in practical development with optocouplers, rectifier. Supplies 15v,9v voltage for positive and negative switches. The isolation is optical- the input stage is an LED and the receiving output is light sensitive (photodetector). It is designed for positive voltage it takes 15v and for negative it takes 9v.

Figure.7. PCB designed Gate driver circuit

Dead-Band Circuit:

Dead band is used to produce a delay time between two switches in same phase of inverter. Fig.8 is designed to produce delay time by utilizing NOT gate. The not gate in this gives complimentary pulse for switch to avoid short circuit of the power supply in the PWM inverters. Dead-band control provides a helpful method for battle current "shoot-through" problems in a power converter. "shoot-through" occurs when both the upper and lower switches in the same phase of a power converter are ON simultaneously, this condition shorts the power supply. Shoot-through issues occur because the switches turn on faster than they turn off. It designed to produce 1m/sec delay.

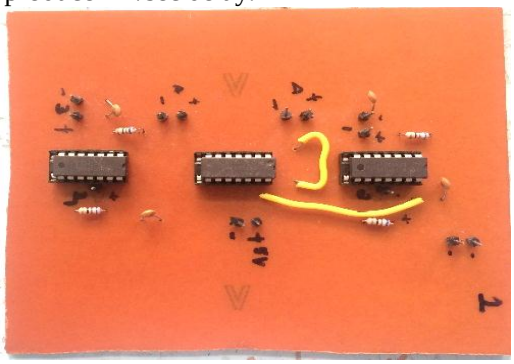

Figure.8. PCB designed Dead-Band circuit

Transformer:

A 230/24v multiple output transformer is designed to obtain isolated supply for the driver circuit of different switches in the inverter. This also reduces too many RPS for supplying voltage. Fig.9 shows the 230/24v multiple output transformer which supplies voltage to gate driver circuits.

Fig.9. Practically designed transformer 230/24v

The table.2 shown is the components data sheet which are included for designing practical three level neutral point clamped inverter.

S.No.	Component	Specification
1	Optocoupler	IC TLP 250
2	AND gate	IC 7408
3	NOT gate	IC 7404
4	Resistors	22 Ω ,390 Ω,70 Ω
5	Capacitors	22 nF, 220 µF, 63 V 1 µF , 63 V
6	Zener Diodes	IN4744A , 1W , 15V IN4740A , 1W , 9V
7	Diodes	IN4007
8	Buffer	IC 7407
9	Transformer	230/24 volts
10	RPS	0-40 volts
11	Mosfets	IRFP250Vdss=200v, Rds=<0.85ohm, Id=33A.

Table.2. components data sheet

6. DSP Description

The open loop system model is developed in practical setup using DSPF28335 with code composer studio, circuit description as specified. Fig.10 shows the generation PWM pulses for NPC inverter Using CCSV4 version the DSP TMS320F28335 is connected to PC. EPWM unit is used to generate six pulses at a time from EPWM pins to DSP. These pulses are given to Opto-coupler with provides opto – isolation between Gate Driver and Switches.

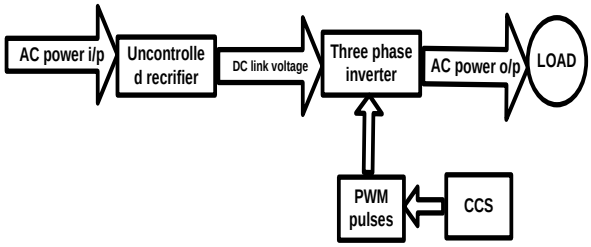

Fig.10. Block diagram for generating PWM pulses using DSP

The pulse pattern can be obtained by connecting a digital oscilloscope. Event manager module contains General Purpose (GP) timers, PWM circuits and output logic, the DSP processor has ePWM output and also has 6 ePWM modules which generates the required PWM signals [8]. For comparison reference signal is 50 hz, the carrier signal switching frequency is 1 KHz. For the generation of PWM signals considering the three phase inverter the following equations are being used.

$$\sin a = \sin\theta \quad (1)$$

$$\sin b = \sin\left(\theta - \left(2\times\frac{\pi}{3}\right)\right) \quad (2)$$

$$\sin c = \sin\left(\theta - \left(4\times\frac{\pi}{3}\right)\right) \quad (3)$$

The above equations based on the amplitude Vm and the phases that is 0, 120 and 240 degree were considered. In ePWM block the carrier wave of required frequency was generated, the counting mode was specified as Up-Down counting. Comparing the combined effect of each of each block, the generated signal was applied to PWM single for each phase. At GPIO00-GPIO11 the PWM pulses are obtained with complimentary and phase shift, the respective result waveforms are shown in below section [9]. Time period is calculated from the following formulae:

$$TBPRD = \frac{1}{2}\times\frac{FSYSCLKOUT}{FPWM\times CLKDIV\times HSPCLKDIV} \quad (4)$$

The PWM pulse generated by DSP is observed in digital oscilloscope is shown in fig.11. the practically developed three level NPC inverter with DSP control board is shown in fig.12.

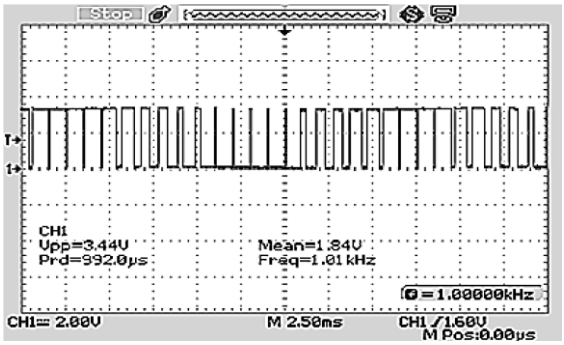

Fig.11. Sine PWM switching pulse at switching Frequency 1 KHz and duty ratio 50%, Sine=50Hz

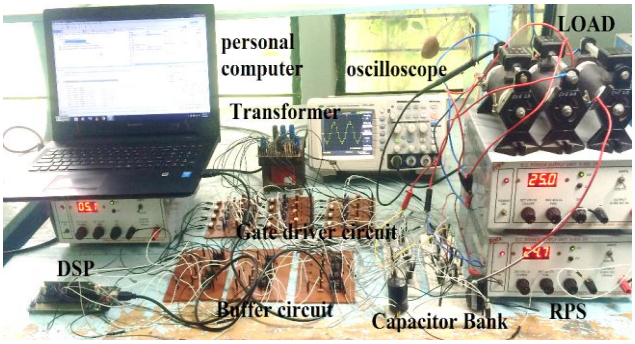

Fig.12. Open loop three level DCMLI inverter in practical

The Proposed technique simulation results at different characteristics compared with conventional sine PWM (SPWM) is observed in oscilloscope are shown in figure (12-19). The conventional SPWM with different loads and power factors are having up to 10v neutral point voltage. The proposed technique with different loads and power factors are having nearly 0v neutral point voltage shown in below figures. It shows the reduction in the neutral point voltage for the proposed technique when compared with sine PWM at different aspects.

In figure (30-35) shows the DSP generated PWM pulses for three phase NPC inverter with complimentary observed in digital oscilloscope with switching frequency 1 KHz. Also three level NPC inverter output voltage is obtained.

7. Results

Simulation Results:

Without feedback

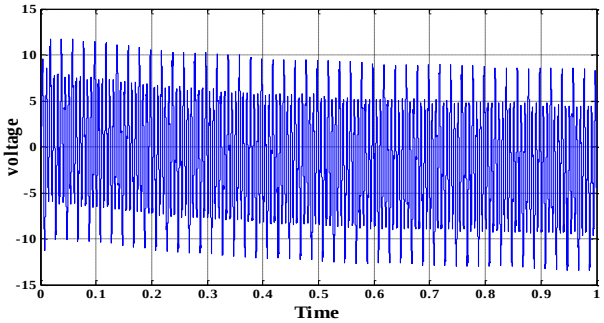

Fig.12. Neutral point voltage with unbalanced load

With feedback

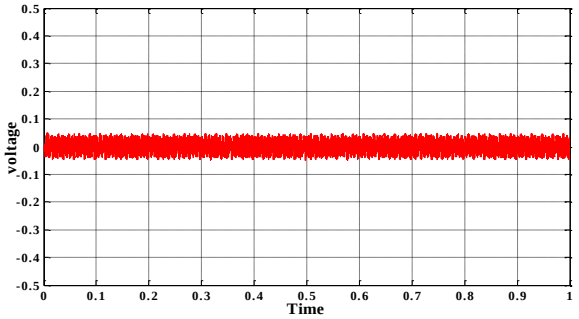

Figure.13. Neutral point voltage with unbalanced load

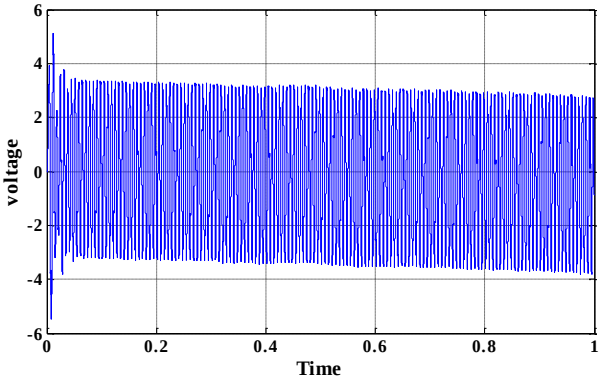

Fig.14. Neutral point voltage at Power factor 0.2

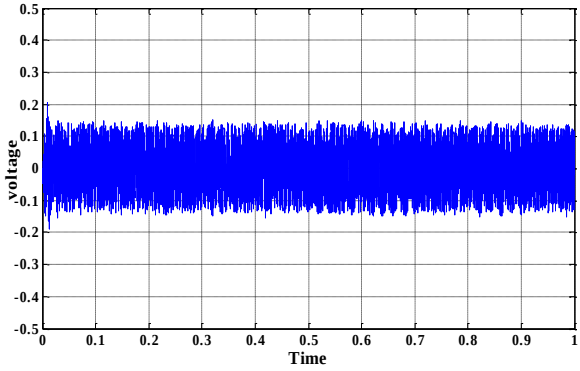

Fig.15. Neutral point voltage at Power factor 0.2

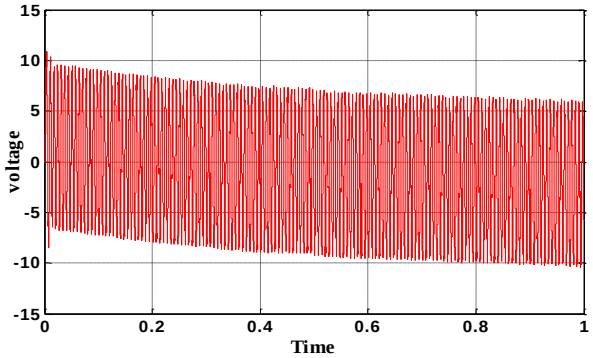

Fig.16. Neutral point voltage at Power factor 0.6

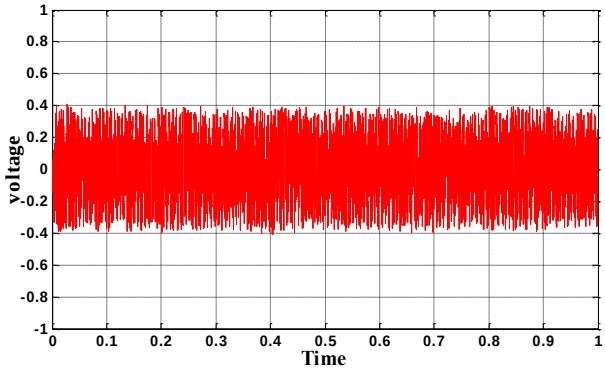

Fig.17. Neutral point voltage at Power factor 0.6

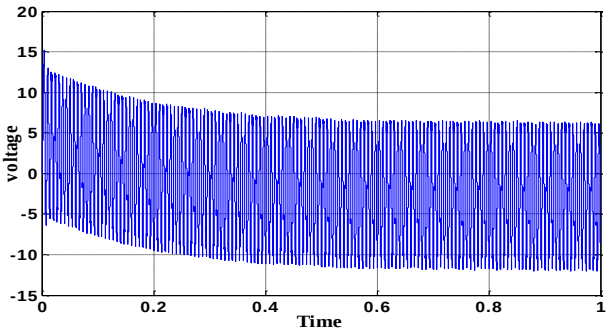

Fig.18. Neutral point voltage at Power factor 0.8

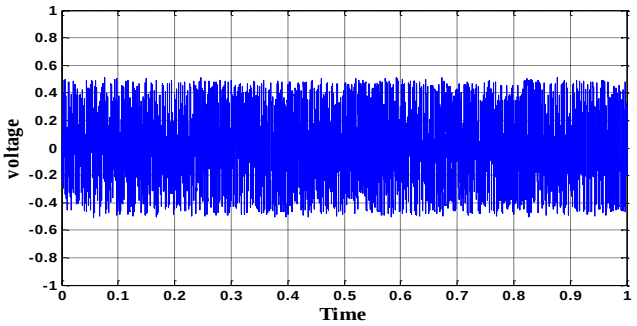

Fig.19. Neutral point voltage at Power factor 0.8

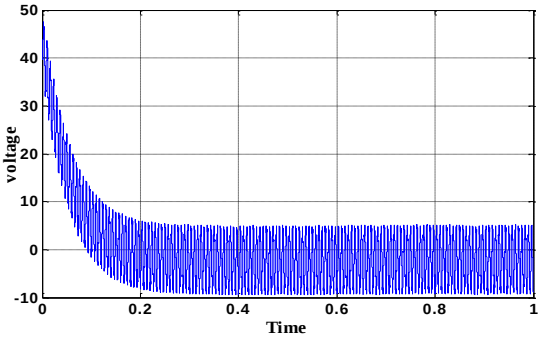

Fig.20. Neutral point voltage when initial voltage of capacitor C1=100v

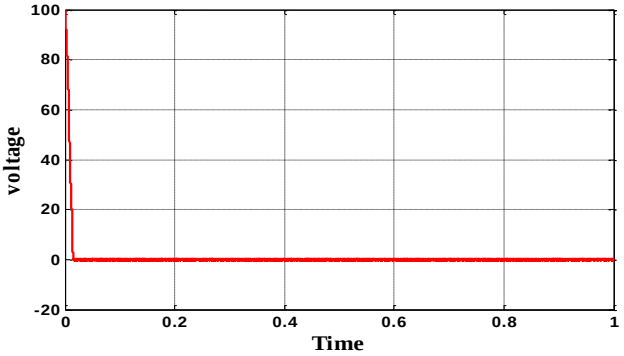

Fig.21. Neutral point voltage when initial voltage of CapacitorC1=100v

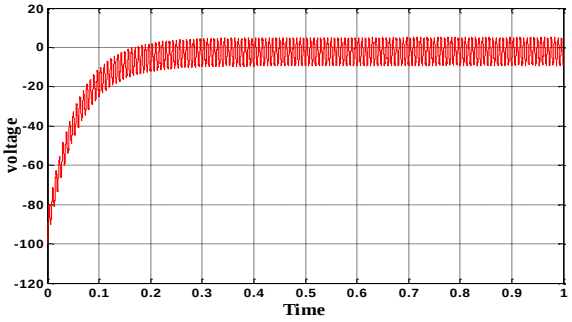

Fig.22. Neutral point voltage when initial voltage of capacitor C1=100v, C2=60v

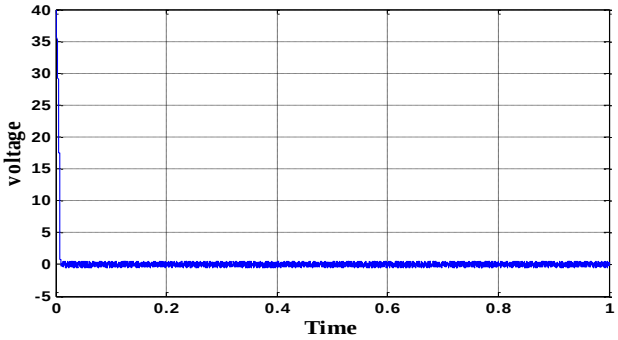

Fig.23. Neutral point voltage when initial voltage of Capacitor C1=100v, C2=60

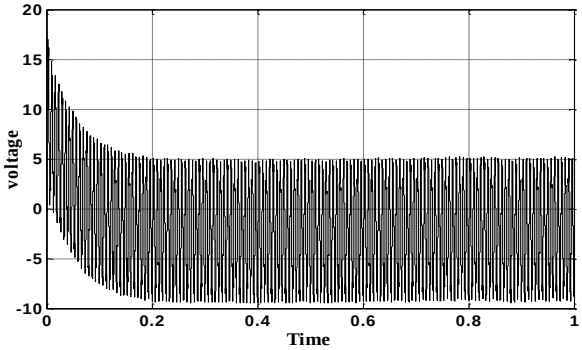

Fig.24. Neutral point voltage with balanced load

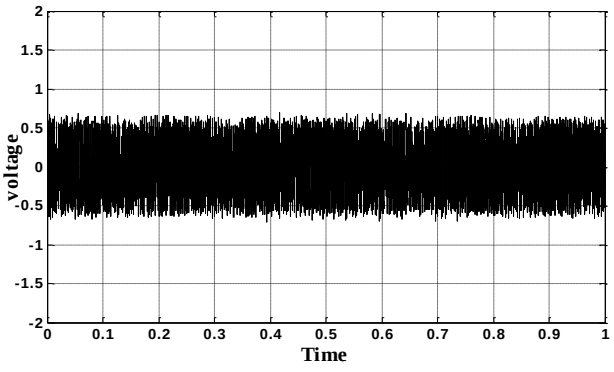

Fig.25. Neutral point voltage at balanced loa

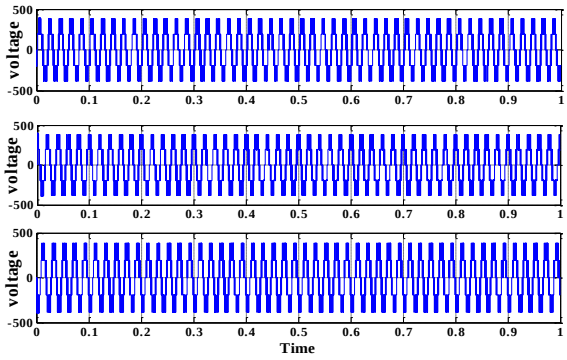

Fig.26. Three level NPC inverter output voltage without Feedback at unity Power factor

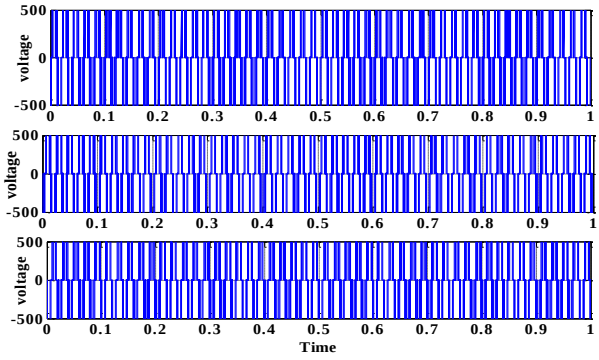

Fig.27 Three level NPC inverter output voltage with Feedback at unity Power factor

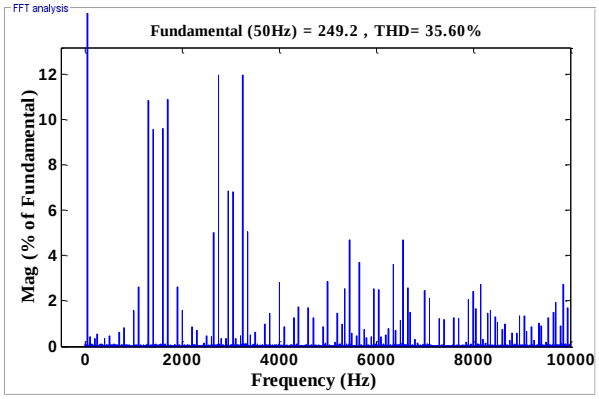

Fig.28 THD analysis of SPWM figure.

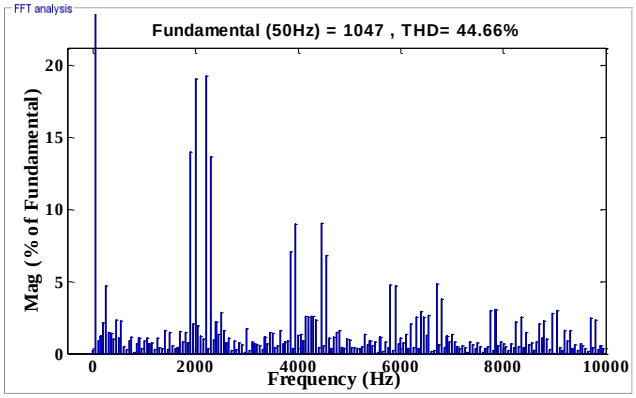

Fig.29. THD analysis of proposed technique

8. Hardware Results

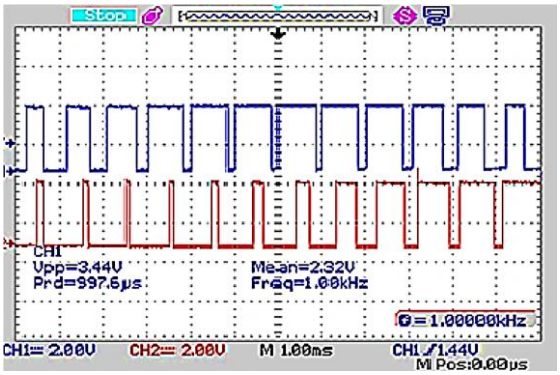

Fig.30. Sine PWM pulses at switching frequency 1 KHz, 1 KHz, Sine=50Hz with phase shift (0^o and 120^o)

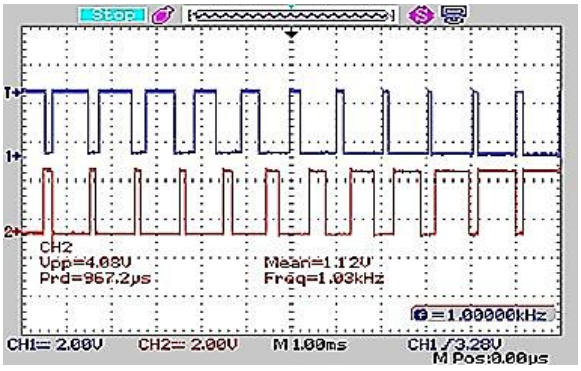

Fig.31. Sine PWM pulses at switching frequency 1 KHz with phase shift, sine=50Hz (0^o and 240^o)

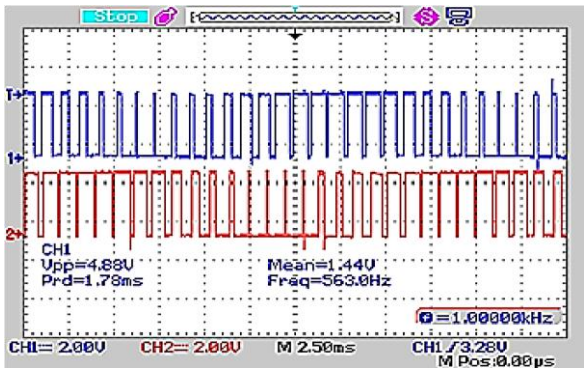

Fig.32. Sine PWM pulses at switching frequency 1 KHz with complementary (ePWM1A and ePWM1B)

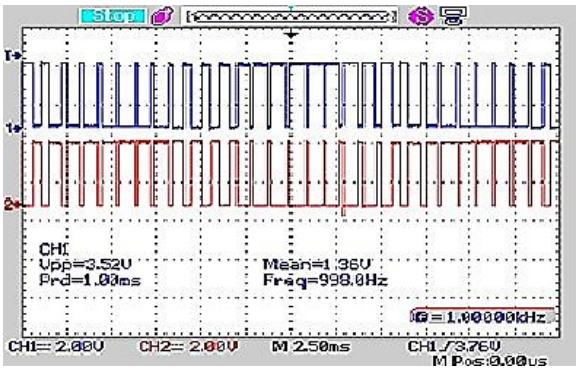

Fig.33. Sine PWM pulses at switching frequency 1 KHz with complementary (ePWM2A and ePWM2B)

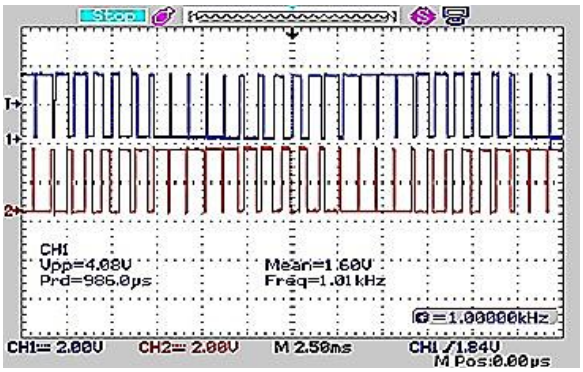

Fig.34 Sine PWM pulses at switching frequency 1 KHz with Complementary (ePWM3A and ePWM3B)

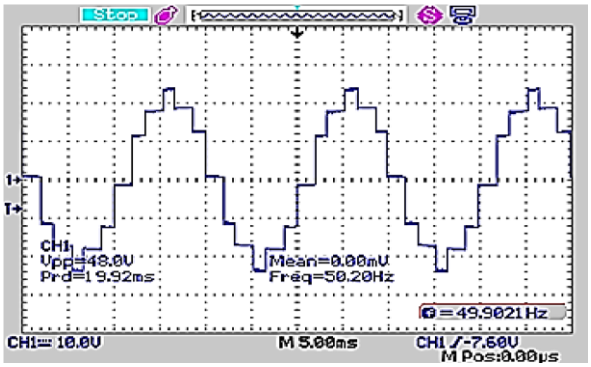

Fig.35. Open loop three level DCMLI output voltage Waveform with three phase R-Load

9. Conclusion

In this paper, design and implementation of proposed technique for Three-level neutral point clamped inverter is presented .It can be observed that neutral point voltage is stabilized for various power factors and loads. It is analyzed that reduction in neutral point voltage of proposed technique is obtained compared with conventional SPWM at different aspects. With the proposed technique inverter efficiency increases, reduces harmonic content in output, neutral point oscillations are Nullified. In practical open loop three level neutral point clamped inverter is developed and tested using DSPTMS320F28335 board with code composer studio. With this 3KW load is developed in the laboratory. Simulation and Practical results are also provided to verify the implementation of approach of Matlab/Simulink and DSP based proposed PWM scheme.

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