FPGA Control of Cascaded Multilevel Inverters: Implementation with Experiments

V.Kumar Chinnaiyan [1], Dr.Jovithajerome [2], J.Karpagam[3]

Abstract— *The main objective of this paper is to design and development of a FPGA based cascaded multilevel inverter with reduced harmonic distortions on the output. Due to the increased usage of power electronic converters for processing the power, the power quality issues become the hot research topic in the recent past. As the power level increases, the voltage level is increased accordingly to obtain satisfactory efficiency. During the last decades, the voltage rating of fast switching high voltage semiconductors such as the Insulated Gate Bipolar Transistor (IGBT) has increased. Still, there is a need for series connection of switching devices. The multilevel power converter has shown growing popularity. The fundamental advantages of the multilevel converter topologies are low distorted output waveforms and limited voltage stress on the switching devices and hence the reduced electromagnetic interferences on the output waveforms. The main disadvantages are higher complexity and more difficult control but it can be overcome by using modern digital controllers. In this work, the performance parameters are analyzed with the developed prototype of a three phase cascaded multilevel inverter designed with digital controller for reduced power quality issues with induction motor drive experimentally with the options to use it for harnessing the renewable energy too. The main focus has been on the quality of output waveform and the result obtained with the developed experimental hardware setup proves the same.*

Keywords —*Power Converters, Power Quality, Cascaded Multilevel Inverter, FPGA, Space Vector Pulse Width Modulation, Loses, Total Harmonic Distortion, Electromagnetic Interferences.*

I. INTRODUCTION

The quality of electrical power has become an important issue for the customers. Customers, in particular, become less tolerant of power quality disturbances because these disturbances degrade the performance and efficiency of customers loads, especially power electronics loads. A recent survey conducted by a utility company showed that more than 80% of the power quality related problems originated with in customer facilities. However, customers usually turn to the local utility to identify the problem. Presently, many utilities maintain dedicated engineers to address customers power quality concerns and to provide appropriate mitigation procedures. In order to to improve the quality of power, electric utilities continuously monitor power delivered at customer sites. Disturbances in waveforms are recorded continuously using power monitoring instruments, producing yearly data files in the gigabyte range. Studies of power quality phenomena have emerged as an important subject in recent years due to renewed interest in improving the quality of electricity supply. As sensitive electronic equipment continues to proliferate, the studies of power quality will be further emphasized.

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Due to rapid change in electrical technologies and environments, many side effects are created. Among these harmonic distortion is one of the most potentially trouble some and unpredictable problems that affect the smooth operation of modern machineries and utilities. In recent years power electronic systems gaining momentum due to their compactness, high efficiency, and in particular multilevel inverters have been an important development in recent years, owing to their capability to increase the voltage and power delivered to the motor with semiconductor switches which are available today [1]-[3]. Because of the stepwise synthesized output waveform of a multilevel converter, a more sinusoidal waveform is generated, creating a number of advantages. The stepwise waveform reduces the *dv/dt* of the output voltage. This can reduce the capacitive currents, and lifetime of cable and motor output voltage. For a drive application a lower *dv/dt* will also reduce the bearing current problems. The reduced voltage distortion will also reduce the current ripple, and hence the need for a output filter will decrease or disappear completely. Also electromagnetic interference concerns are reduced.

Multilevel inverters have gained growing popularity in high-power drives because of low switching losses and harmonic distortions in the output voltage [4]. Various inverter topologies, like Neutral Point Clamped (NPC), cascaded H-bridge, and flying-capacitor-based multilevel inverter topologies, are being used for adjustable-speed-drive applications [3]. The harmonic components has the frequencies that are integer multiples of the system fundamental frequency. Adjustable Speed Drive (ASD) system is disturbing power quality by generating harmonics and inter-harmonics. Pulse Width Modulation (PWM) technique is one of the techniques used to mitigate the harmonics in ASD [4]. There are several PWM techniques available for the control of ASD system. Normally, PWM technique is used to generate the required voltage or current to control ASD system. With the development of Digital Signal Controllers [5], Space Vector Modulation (SVM) has become one of the most important PWM methods for three phase power converters. SVM is the most widely used technique for AC drives with the condition that the harmonic current is as small as possible and the maximum output voltage is as large as possible[6]. It uses the space vector concept to compute the duty cycle of the power switches. Easy digital implementation and wide linear modulation range for output line to line voltages are the notable features of space vector modulation [6]-[8]. SVM involves switching between the three nearest space vectors from the available states of an inverter [11]. Several approaches have been presented to show how these space vectors can be selected for particular operating conditions. SVM is best suited for the harmonics reduction on the output waveforms

compared to PWM techniques where the flexibility for fine tuning is very limited [11].

Advantages of SVM over PWM techniques are

- Line to line voltage amplitude can be as high as V_{DC}. Thus 100% VDC utilization is possible in the linear operating region.
- In the linear operating range, modulation index range is 0.0 to 1.0 in the sine PWM, where as in the SVM, it is 0 to 0.866. line to line voltage amplitude is 15% more in the SVM with the modulation index=0.866, compared to the SPWM with modulation Index = 1. Hence it has the better usage of the modulation index depth.
- With the increased output voltage, the user can design the motor control system with reduced current rating, keeping the horse power rating at the same level. The reduced current helps to reduce the inherent conduction loss of the VSI.
- Only one reference space vector is controlled to generate the three phase sine waves.
- Implementation of SVM switching rules gives less THD and less switching loss.
- Flexibility to select inactive states and their distribution in switching time periods gives two degrees of freedom.

With the advent of modern digital processors with high operating speed and memory capacity it is easy to implement the complex algorithm with single controllers with least accessories. For applications such as ac motor drives, it is desirable to minimize the harmonics and inter harmonics voltage to prevent premature bearing failure and reduce EMI levels keeping these objectives the hardware is developed and integrated for testing. The software algorithm is fine tuned for the lower percentage of THD on output waveforms [12].

II. HARDWARE IMPLEMENTATION OF THREE PHASE CASCADED MULTILEVEL INVERTER

A 5 kVA prototype using IGBT (600V, 50A) has been built in order to verify the proposed three phase five level cascaded multilevel inverter as shown in figure 1. The load is a three-phase induction motor, which is loaded less than 1.0kW. A Xilinx Spartan XC3S400 FPGA controller is used to implement the control algorithm and generates the firing pulses for power switches which supply the power to drive the motor with the real-time computations[9].

The complete hardware specification of the proposed system is as follows, input supply is any one of the following ratings 415/430V, Three Phase 50Hz AC Supply or the isolated photovoltaic panels with 60V output DC or storage batteries with the combination of producing 60V output DC. The output system specifications are 5kVA, 415V,15A, 50Hz, Three Phase AC supply confined to IEEE/EN50160 Standards (like %THD <5%, Unity Power Factor, permissible Voltage sags and swells, frequency deviations and etc.,). The proposed control algorithm is generated in the front end with the aid of system generator editor, the SVM blocks with the necessary transformation equations and the associated blocks for individual phases are interconnected and the sampling frequency is set to 5kHz[10]. The entire control algorithm based on SVM is developed in the system generator environment and downloaded into the FPGA processor and the switching pulses are obtained for the power switches.

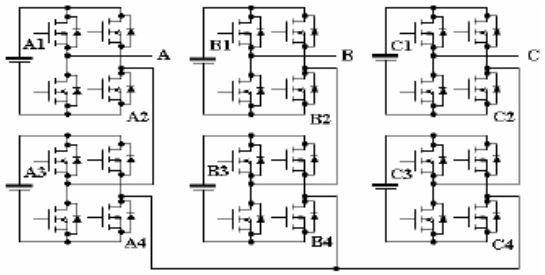


Fig. 1: Three Phase Five Level Cascaded Multilevel Inverter

A Field Programmable Gate Array (FPGA) is a high performance data processing general-purpose integrated circuit digital controller that is "programmed" by the designer rather than the device manufacturer. Unlike an Application Specific Integrated Circuit (ASIC), which can perform a similar function in an electronic system, an FPGA can be reprogrammed, even after it has been deployed into a system [5]. A FPGA is programmed by downloading a configuration program called a bitstream into static on-chip Random-Access Memory (RAM). Much like the object code for a microprocessor, this bitstream is the product of compilation tools that translate the high level abstractions produced by a designer into something equivalent but low level and executable. An FPGA is similar to a Programmable Logic Device (PLD), but whereas PLDs are generally limited to hundreds of gates, FPGAs support thousands of gates. They are especially popular for prototyping integrated circuit designs for power electronics applications.

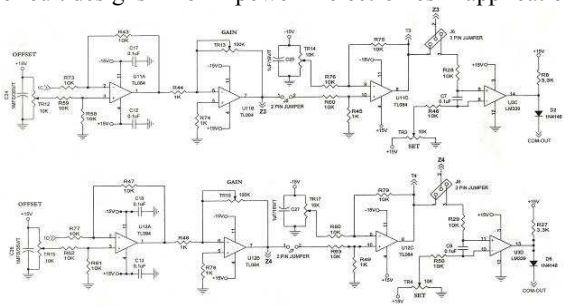


Fig. 2: Amplification circuit between the FPGA and Power Circuit

The output pulses obtained from the FPGA ports are at the level of 3.5V DC which is insufficient to turn ON the power switches, Hence with the aid of operational amplifiers the signal is amplified to the level of 12V, which is sufficient to turn ON the power switches. The input, output terminals and the associated components for the amplification card is as shown in figure 2.

In order to protect the power devices and the connected loads from the damages the phase currents and the neutral current are continuously sensed with the aid of LEM make Current Transducer LTS 25-NP whose primary current ratings are I_{PN} = 8 - 12 - 25 A, it can be used to measure currents of DC, AC, pulsed, mixed, with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit). It is a Closed loop (compensated) multirange current transducer using the

Hall effect, unipolar voltage supply, insulated plastic case recognized according to UL 94-V0, Compact design for PCB mounting, Incorporated measuring resistance, Extended measuring range.

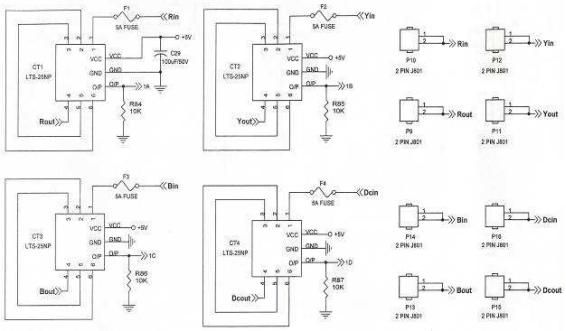


Fig. 3: Current sensor for protection of power switches

The advantages are excellent accuracy, Very good linearity, Very low temperature drift, Optimized response time, Wide frequency bandwidth, No insertion losses, High immunity to external Interference, Current overload capability. The sensor circuit used for hardware implementation with necessary components and their connections is as shown in figure 3.

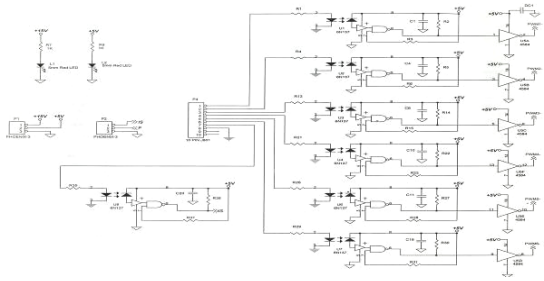


Fig. 4 : Isolation circuit between the controller and power circuit

In any power electronics system the main problem is isolating the power circuit from the control circuit. There are many situations where signals and data need to be transferred from one subsystem to another within a piece of electronic equipment, or from one piece of equipment to another, without making a direct Ohmic electrical connection. Often this is because the source and destination are (or may be at times) at very different voltage levels, like a microprocessor which is operating from 5V DC but being used to control a TRIAC which is switching 240V AC. In such situations the link between the two must be an isolated one, to protect the microprocessor from overvoltage damage. Relays can of course provide this kind of isolation, but even small relays tend to be fairly bulky compared with ICs and many of today's other miniature circuit components. Because they are electro-mechanical, relays are also not as reliable and only capable of relatively low speed operation. Where small size, higher speed and greater reliability are important, a much better alternative is to use an optocoupler. These use a beam of light to transmit the signals or data across an electrical barrier, and achieve excellent isolation. Here the opto-isolator 6N137 is employed. The diode can be used in a photovoltaic mode or a photoconductive mode. In photovoltaic mode, the diode acts as a current source in parallel with a forward-biased diode. The output current and voltage are dependent on the load impedance and light intensity. In photoconductive mode, the diode is connected to a supply voltage, and the magnitude of the current conducted is directly proportional to the intensity of light. The complete setup of the isolation circuit used for the hardware implementation is as shown in the figure 4.

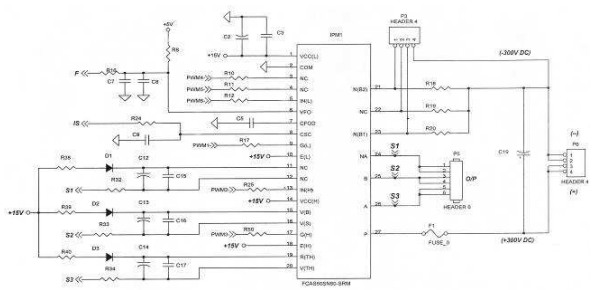


Fig.5: Connection Diagram for FCAS50SN60 Smart Power Module for Cascaded Multilevel Inverter

FCAS50SN60 is an advanced smart power module for motor drive that Fairchild has newly developed and designed to provide very compact and high performance motor drives mainly targeting medium power inverter-driven ac drive applications especially for industrial applications. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. In addition the incorporated HVIC facilitates the use of single-supply drive topology enabling the FCAS50SN60 to be driven by only one drive supply voltage without negative bias. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

The figure 5 shows the connection of a single smartpower module, similar setups were used for other five smartpower modules to obtain the five level power circuit configuration.

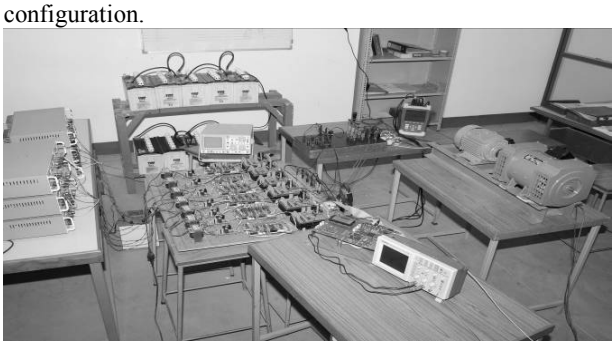


Fig. 6: Complete hardware setup with measuring equipment and loading arrangements

III TESTING OF EXPERIMENTAL SETUP AND DISCUSSIONS

After the modular design of various units, each module was tested carefully and integrated to achieve the stated performance of the system. The complete hardware setup with necessary provisions for testing and waveform observations are shown in figure 6. The provision such as to feed the input from three phase AC supply, Storage batteries and also from the solar panels are also made on the developed system. Necessary arrangements like isolated supply, PC interfacing for online monitoring and the provision for varying the load were made and the

photographs shown above are depicts the same. In order to have smooth variations on the load, the developed system drives the three phase Induction motor load coupled with a DC shunt generator whose specifications are given in the appendix.

In order to load the three phase induction motor a DC generator is mechanically coupled to it and the DC generator is loaded with the resistive load and this setup constitutes the loading arrangements for the developed hardware. This setup provides a linear load variation on the inverter side and the performance parameters such as terminal voltage, current and harmonics for the output frequencies of 40Hz, 45Hz and 50Hz are captured with the aid of Fluke make three phase power quality analyzer. Here the Fluke 434 model is used, it is a three phase power quality analyzer, it complies with the following international standards, ANSI/ISA S82.01-1994, EN/IEC61010-1 2nd edition 1000V measurement category III, 600V Measurement Cat IV, Pollution degree 2,CAN/CSA-C22.2 No.61010-1-04. The power quality analyzer is suitably configured in order to obtain the waveforms and tabulations during the testing process.

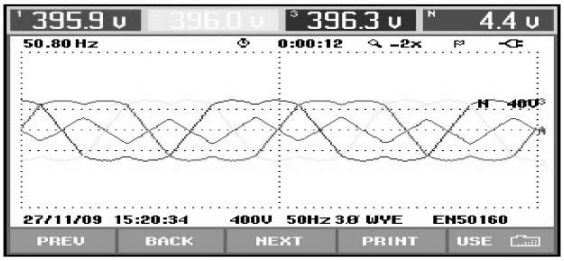


Fig.:7 Three phase output waveforms captured using power quality analyzer in scope mode

The nominal voltage is set as 400V and the power quality limits used is EN50160, the voltage and current probes are set with the appropriate limits to acquire the waveforms.

The developed system is connected to the three phase ac motor i.e. loading arrangements and the readings are captured with the aid of power quality analyzer in the scope mode and the three phase output voltage waveform is as shown in the figure 7 for the set frequency of 50Hz on the digital processor. The output voltages in all the phases i.e. RYB are 396V and the phases are 120^0 apart from each other. The neutral potential is also with in the prescribed limits. Figure 8 shows the associated load current waveforms when the motor is loaded with 33% of rated load, waveforms are captured for the set frequency of 40Hz.

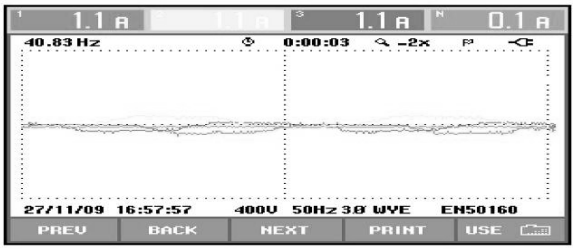


Fig.:8The load current waveforms with the set frequency of 40Hz

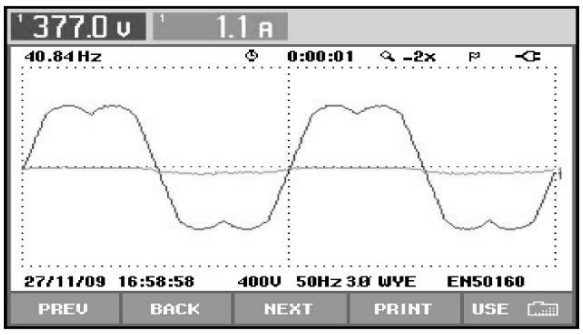


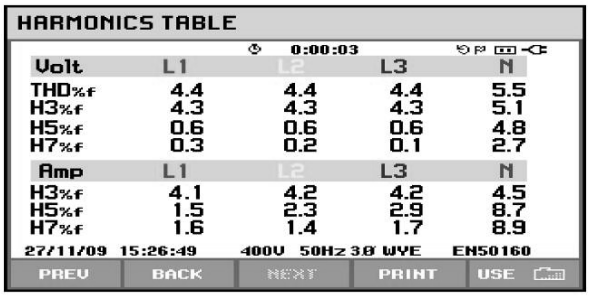
Fig.:9 output waveforms for R phase with the set frequency of 40Hz

The figure 9 shows the output voltage waveform for the R phase with the set frequency of 40Hz. The harmonics of the output voltage and the current harmonics are also listed in the harmonics table of the analyzer as shown in table I. The table shows that the harmonics are very well with in the limits of the power quality standards and hence the developed system performance is at par with the standards prescribed for the same.

The Total Harmonic Distortion (THD) profile of the output waveform is also obtained with the power quality analyzer and the same is as shown in figure 10. In order to check the pattern of the output pulses, it is captured using digital storage oscilloscope and the pulses are as shown in figure 11. Similarly the pulses are tested for all the modules before applying it for the power switches.

Figure 12 shows the waveform with the five levels which is obtained at the R phase output of the developed hardware setup across the load using the digital storage oscilloscope. Figure 13 shows the output line to line voltage waveforms when the motor is running at rated speed with the supply frequency of 50Hz.

Table I Output harmonics table obtained during testing with power quality analyzer



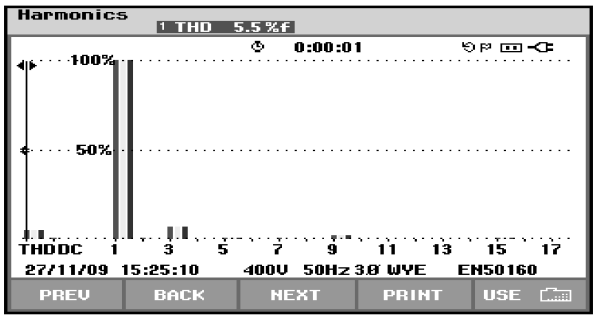


Fig.:10 THD profile of the developed system under test conditions

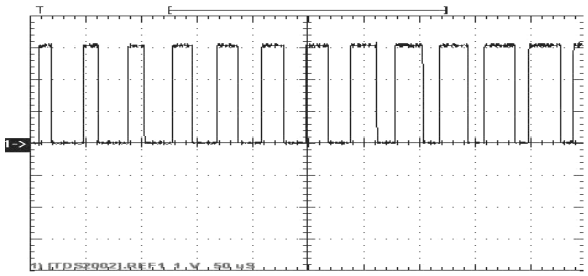


Fig.:11 Triggering Pulses for power switches from FPGA processor

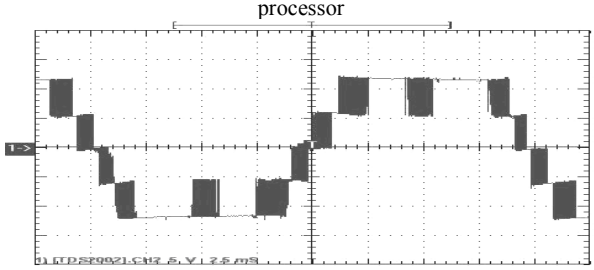


Fig.:12 Five level output voltage capture using Digital torage oscilloscope

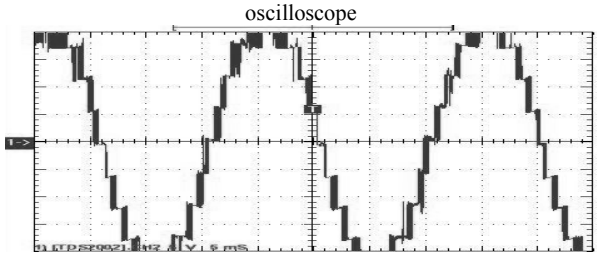


Fig.:13Five level line to line voltage across the three phase induction motor terminals

IV CONCLUSION

This article discussed the implementation and performance testing of a low cost FPGA based cascaded multilevel inverter for induction motor drive with reduced total harmonic distortion. The main advantage of this is the ability to generate SVPWM waveform generation in real time using the control algorithm embedded in the Xilinx processor. This reduces the computation time, required to determine the switching times for inverter legs, making the system suitable for real-time implementation for larger drives where as the power quality issues are the major considerations which adversely affects the performance of motor drives. Furthermore during the testing of the output of the developed experimental setup with the fluke 434 model three phase power quality analyzer shows that the results exhibits the good quality of output waveforms with higher fundamental component and also that the power quality issues are very well with in the limits. The results from the experimental setup show the output waveforms for reduced percentage THD and EMI. The higher fundamental component on output results in reduced switching losses in semiconductor switches as well as on the motor drive. With these results a conclusion can be, the conventional drives with two level inverters can be replaced with multilevel inverter where ever it is possible in order to maintain the good quality of the power in addition to the quantity on the common grid in the years to come.

APPENDIX

The following are the specifications of the machines used for the experiment: Induction Motor : Kirlosakar make, Three Phase Star Connected, 1.5kW, 415V, 3.35A, duty Cycle S1,50 Hz, Nr =1400 rpm, four poles, Rs = 1.98 Ω, Rr = 3.69 Ω, M = 0.232 H, Ls = 0.26 H, Lr = 0.25 H, J = 0.1 kg · m^2, and B = 0.01 N m/s. DC Generator Benn Make Shunt Type,1.0kW,220V,4.6A,1500RPM, Duty Cycle CMR

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