INVESTIGATIONS ON NEW THREE PHASE MULTILEVEL INVERTER WITH REDUCED SWITCHES

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Abstract: *This paper presents a new three phase seven level inverter with sinusoidal reference and trapezoidal reference for various Pulse Width Modulation (PWM) strategies like Phase Disposition (PD), Phase Opposition and Disposition (POD) PWM, Alternative Phase Opposition and Disposition (APOD) PWM, Carrier Overlapping (CO) PWM and Variable Frequency (VF) PWM. This paper compares various performance indices like Total Harmonic Distortion (THD), V_{RMS} and V_{PEAK} for various modulation indices with sine and trapezoidal reference. The chosen multilevel inverter uses only eight switches while compared conventional multilevel inverter. The performance of proposed work is simulated through MATLAB/SIMULINK. It is observed that COPWM strategy perform better since it provides relatively higher fundamental RMS output voltage.*

Key words: *PWM, THD, COPWM, Reduced switch, three phase*

1. Introduction.

A MultiLevel Inverter (MLI) is relatively used in high voltage and high current applications. The desired stepped AC voltage waveform is obtained from several levels of DC voltage. It provides more advantages as compared with conventional two-level inverter because it provides lesser switching losses and frequency. The smallest number of voltage/current levels for a multilevel inverter is obtained using cascaded inverter. When the number of levels increases the THD obtained will be close to zero. The attained number of voltage levels however faces voltage unbalance problems, circuit setup, packaging restraints, initial and maintenance cost. Waltrich et al. (2010) proposed a modular three-phase multilevel inverter mainly applicable for electrical drive applications. Unlike the cascaded H-bridge inverter, this topology is depending upon power cells connected in cascade using two inverter legs in series. Malinowski et al. (2010) presents cascaded multilevel inverters which allows one to achieve high quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Lezana et al. (2011) introduce a hybrid multi-cell converter in which allows that no losses and high modularity. Floricau et al. (2011) proposes new multilevel converters based on stacked commutation cells with shared power devices. Kangarlu et al. (2012) discusses a symmetric multilevel inverter with reduced components based on non-insulated DC voltage sources. Yousedfpoor et al. (2012) discusses an efficient approaching to reduce the harmonic contents of the inverter's output voltage by THD minimization. Rathore et al. (2013) proposes an optimal pulse-width modulation of multilevel inverters for low-switching-frequency control and for harmonic control. Odeh et al. (2013) discusses a switching cycles which optimize through analysis, the harmonic distortion of the inverter output line voltage waveforms have been decreased. Kui Wang et al. (2013) made a new five-level inverter which can get overcome the limitations of traditional neutral-point-clamped and flying capacitor converters. It can be naturally balanced beneath ideal and steady conditions. Ajami et al. (2014) introduce a cascade multi-cell multilevel converter and it has one advantage that to reduce THD. Buccella et al. (2014) propose a procedure to eliminate harmonic components from inverter output voltage and, for each harmonic, return the exact boundaries of all valid modulation index intervals. Dayoodnezhad et al. (2014) present the strategy uses the measured average of the switched phase leg output voltage to adjust the controller hysteresis band as the load back Electro Motive Force (EMF) varies to maintain a near constant phase leg switching frequency.

Hence this paper presents a new seven level inverter which uses eight power switches. Output voltages are phase voltage V_P and line voltage V_L.

2. Proposed Multi Level Inverter

Multilevel inverter is a power electronic device which synthesis an AC voltage from desired sinusoidal waveform and which actually divides the main DC supply to separate DC voltage sources. The proposed symmetrical multilevel inverter consists of three DC voltage sources (E_1, E_2 and E_3) and eight power semiconductor switches with three phase Resistive (R) load. Three DC voltage sources are, $E_1=E_2=E_3=V_{dc}$ and R- load has 100Ω. Proposed MLI needs only eight switches, but for Conventional Cascaded MultiLevel

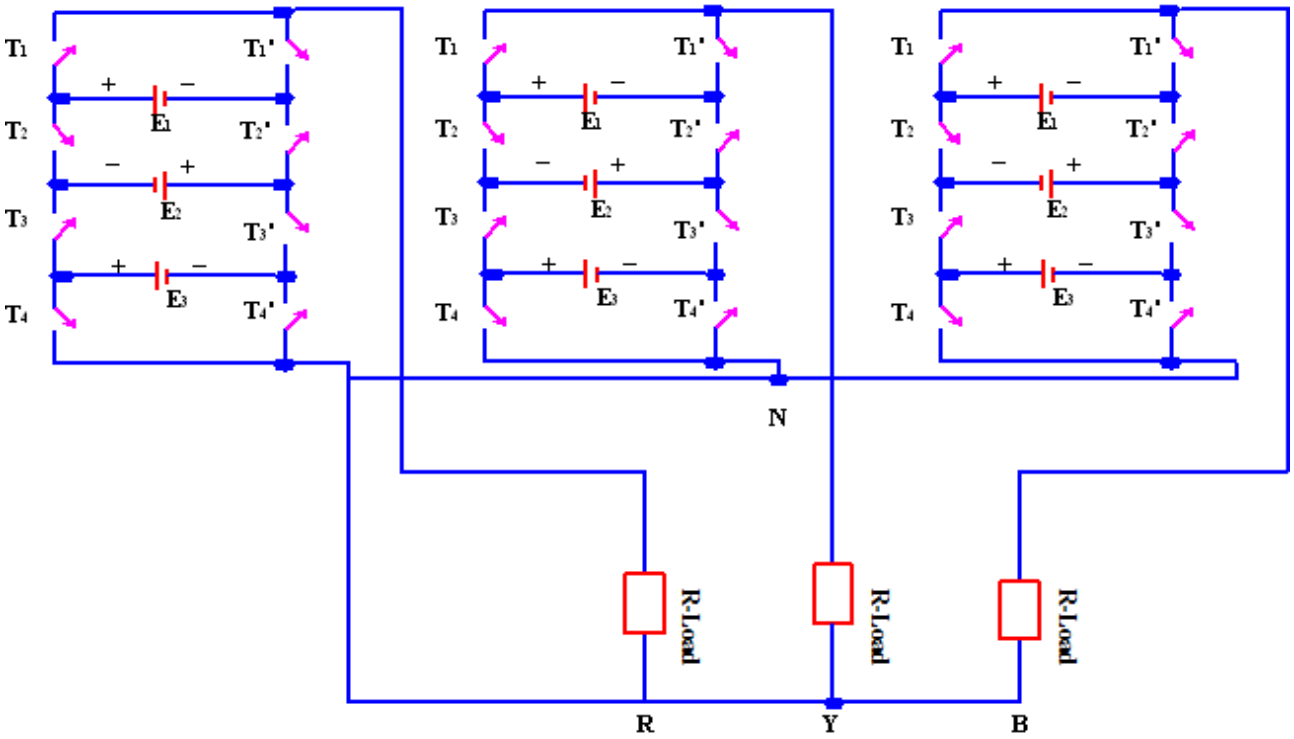

Fig. 1. Proposed three phase seven level inverter.

Inverter (CMLI) contains twelve switches to generate symmetrical seven level output. A different mode of operation is used to generate different switching patterns.

Bipolar PWM strategies are used to compare the performance measures for both reference waveforms. Trapezoidal reference is comes under advanced modulation technique while compared with sine reference waveform. The Eight switches used are T_1, T_2, T_3, T_4, T1', T_2', T_3' and T_4'. The bi-directional switches used are Metal Oxide Silicon Field Effect Transistor (MOSFET), Insulated Gate Bi-polar Transistor (IGBT) and etc., The seven level output voltages are $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, $0V_{dc}$, $-3V_{dc}$, $-2V_{dc}$ and $-V_{dc}$. This seven DC voltages produces stepped or staircase waveform from an approximate AC sinusoidal waveform. All performance measures are obtained for both line voltage and phase voltage separately.

The operations of different switching states are as shown: For $+3V_{dc}$ output switches T_1, T_3, T_3 and T_4' should be in ON position. For $+2V_{dc}$ output switches T_1, T_3, T_4 and T_2' should be in ON position. For $+V_{dc}$ output switches T_1, T_2', T_3' and T_4' should be in ON position. Same as for $0V_{dc}$ output switches T_1', T_2', T_3' and T_4' should be in ON position. The negative polarity output voltages $-3V_{dc}$, $-2V_{dc}$ and $-V_{dc}$ are redundancy for positive polarity output voltages. MLI has applications in the area of adjustable speed drives and renewable energy sources (solar cell, Fuel cell, wind energy and etc.).

Figure 1 shows proposed three-phase seven-level inverter with three-phase Y (star) connected resistive load. Therefore, to obtain the total AC voltage by the multilevel inverter, there are seven distinct AC voltage levels that are to be added together.

The load voltage is equal to the summation of the output voltage of the three-legs that are connected in series. The magnitude of DC input Voltage V_{dc} was set as 50V and the load used is Resistive $R_L = 50\Omega$. The voltage stress on each switch is decreased. Therefore, the rated voltage and consequently the total inverter power could be safely increased by increasing the resistive load value.

Three input DC sources with $E_1 = E_2 = E_3 = 50$ V are used. The switching table is shown in Table 1, which shows that switches T_2, T_2', T_3 and T_3' operate at a fundamental frequency of 50 Hz while switches T_1, T_1', T_3, and T_3' operate at a frequency of 2 kHz. Thus, low-voltage-rated switches operate at high frequency and incur more switching losses, while high-voltage rated switches operate at fundamental frequency and incur more conduction losses. In this manner, the total losses among the switches get distributed. Switching losses are very directly proportional to the switching frequency. This paper evaluates THD, V_{RMS} and V_{PEAK} for both line voltage and phase voltage. Comparison of THD and RMS fundamental output voltage for sine and trapezoidal references can also be determined through FFT analysis.

Table 1. Switching Table for proposed seven level inverter.

S. No.	Switching States								Output Voltage
	T_1	T_2	T_3	T_4	T_1'	T_2'	T_3'	T_4'	
1	1	0	1	0	0	1	0	1	$+3V_{dc}$
2	1	0	1	1	0	1	0	0	$+2V_{dc}$
3	1	0	0	0	0	1	1	1	V_{dc}
4	0	0	0	0	1	1	1	1	0
5	0	1	1	1	1	0	0	0	$-V_{dc}$
6	0	1	0	0	1	0	1	1	$-2V_{dc}$
7	0	1	0	1	1	0	1	0	$-3V_{dc}$

3. Switching Scheme.

High-switching-frequency modulation methods like multicarrier bipolar PWM and space vector modulation techniques have been used for MLI modulation control. This proposed topology can be modulated with any one of these methods with suitable adjustment. In the present work, the multicarrier bipolar PWM scheme is used. In a multicarrier bipolar PWM scheme, carrier signals are compared with the reference signal, and the pulses obtained are used for switching of devices. In this proposed topology, one switch may contribute for synthesis of more than one level at output terminals.

Development of this PWM technique is used to reduce the THD of the output. When increasing the switching frequency of the PWM pattern, it can reduce the lower frequency harmonics due to move away the switching frequency carrier harmonics and sideband harmonics from the fundamental frequency component.

The modulating/reference wave of multilevel carrier based PWM strategies can be sinusoidal PWM signal. The reference wave is concerned for CFD including frequency, amplitude and phase angle of the reference wave. This switching table will lead to fundamental switching of T_2, T_2', T_3 and T_3' which bear voltage stress of 2Vdc each as compared to the remaining switches which bear voltage stress of V_{dc} each. This treatment can, however, be extended for higher level inverters. In this various Bipolar PWM techniques but for only two sample techniques Bipolar Phase Disposition (BPD) PWM and Bipolar Variable Frequency (BVF) PWM are used. Because this technique generate reduced total harmonic distortion.

Bipolar multicarrier techniques with sine reference are as given: In Phase disposition technique, all the carriers are in phase with each other. For an m-level inverter using bipolar multicarrier technique, (m-1) carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is ended at zero level. The three-phase sine reference wave is continuously compared with each of the carrier signal. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices would be switched off. The frequency ratio m_f is defined in the PWM strategy as follows:

$$m_f = \frac{f_c}{f_m}$$

The amplitude modulation index m_a of this method is

$$m_a = \frac{A_m}{n*A_c}$$

Figure 2 shows the multicarrier arrangement for PDPWM method for $m_a = 0.9$ and $m_f = 40$.

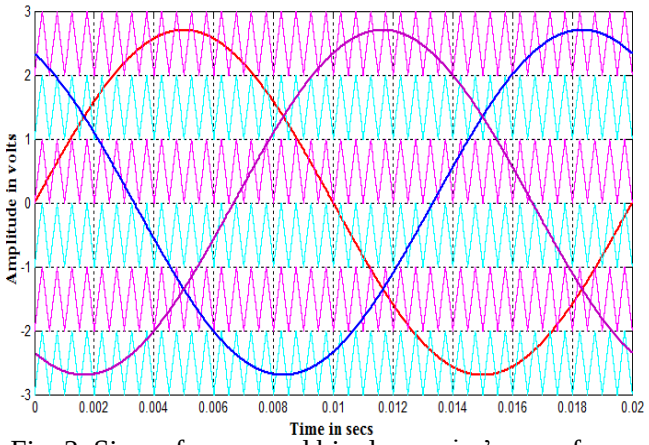

Fig. 2. Sine reference and bipolar carrier's waveform for the proposed scheme with a seven level output.

In Variable Frequency technique, use of six carrier signals with same amplitude and variable frequency to generate seven level output. The number of switching for above and below devices of chosen MLI is much more modulation than intermediate switches. This technique also has same amplitude modulation index m_a as PDPWM technique. Figure 3 shows the multicarrier arrangement for VFPWM method for $m_a = 0.9$ and $m_f = 40$.

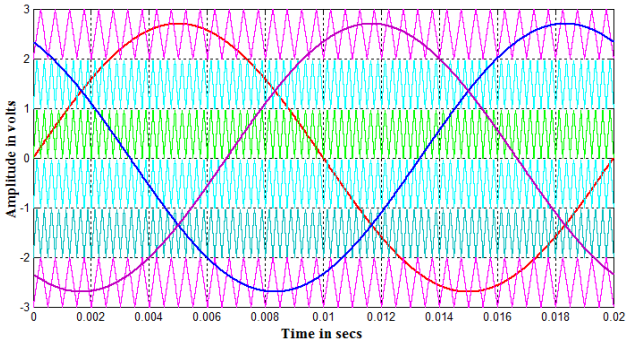

Fig. 3. Sine reference and bipolar carrier's waveform for the proposed scheme with a seven level output.

The PWM technique (Fig. 4) is similar to sinusoidal reference except the reference is replaced. Figure 3 shows the multicarrier arrangement for PDPWM method for $m_a = 0.9$ and $m_f = 40$.

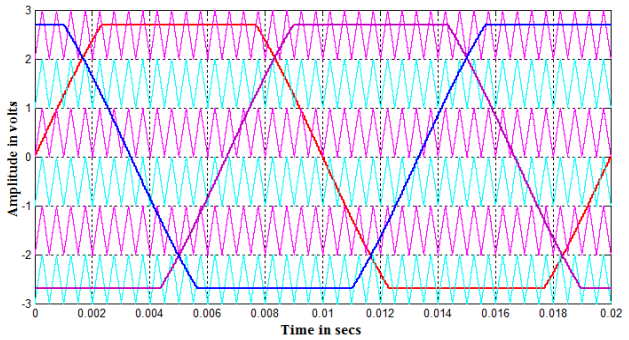

Fig. 4. Trapezoidal reference and bipolar carrier's waveform for the proposed scheme with a seven level output.

Trapezoidal reference with Bipolar VFPWM technique is same as sine reference with bipolar VFPWM technique. Figure 5 shows the multicarrier arrangement for VFPWM method for $m_a = 0.9$ and $m_f = 40$.

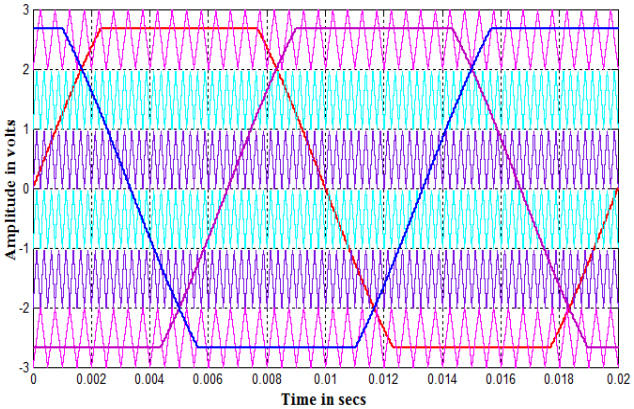

Fig. 5. Trapezoidal reference and bipolar carrier's waveform for the proposed scheme with a seven-level output.

4. Simulation Results

The three phase cascade seven level inverter can be modeled in SIMULINK model by using power system block set. Switching signals for Cascaded Multi Level Inverter (CMLI) are developed using BPWM techniques. The proposed techniques are BPDPWM and BVFPWM with sine and trapezoidal reference. The power balancing among input DC sources is important so that all DC sources have equal lifetimes. Power balancing is also crucial when the DC sources are renewable sources such as PV cells.

For a CHB (Cascaded H-Bridge) inverter with multiple inputs DC sources carrier rotation scheme is employed for equal utilization of sources. Power balancing can be achieved if sources E_1, E_2 and E_3 are utilized alternately in full cycles of the output waveform and balancing can be achieved in two cycles.

The simulation is performed for different values of m_a ranging from 0.7-1. The corresponding % THD values, V_{RMS} of fundamental and peak amplitude voltage V_{PEAK} of inverter output for same modulation indices are shown in below tables. Figs.6 -21shows the simulated output waveforms for both the phase voltage and line voltage for a CMLI and its corresponding FFT plots but for only sample value of $m_a = 0.9$. Tables. 2 – 12 display the performance measures such as %THD, V_{RMS} and V_{PEAK}. Figures. 6 – 21 shows the three-phase output voltage (phase voltage and line voltage) waveforms for sine and trapezoidal references and its respective FFT plots.

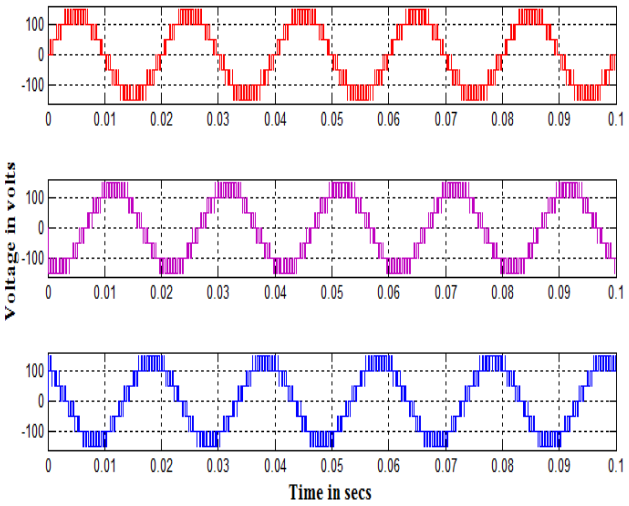

Fig. 6. Three phase output waveform for phase voltage V_P with sine reference.

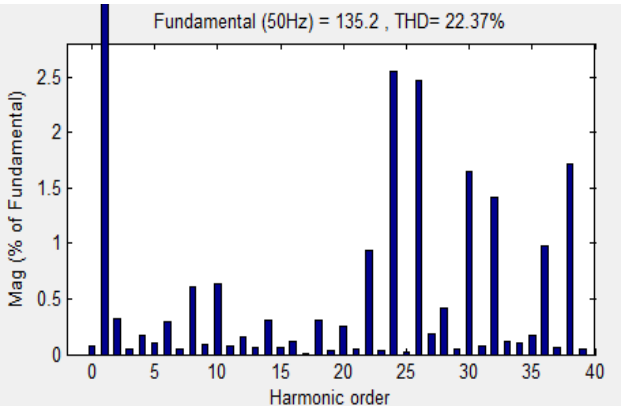

Fig. 7. FFT plot for phase voltage of BPDPWM technique with sine reference.

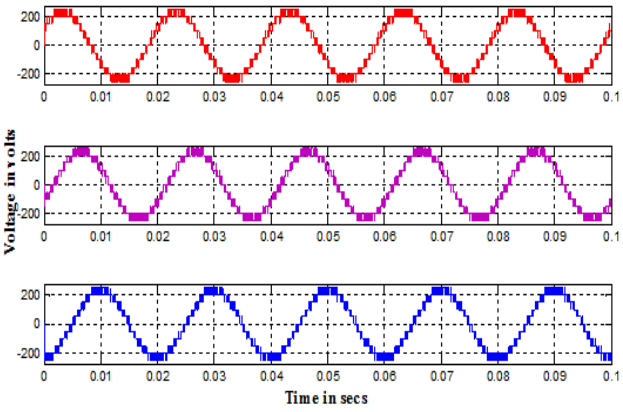

Fig. 8. Three phase output waveform for line voltage V_L with sine reference.

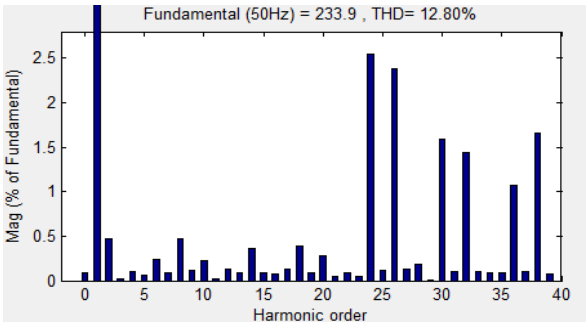

Fig. 9. FFT plot for line voltage of BPDPWM technique with sine reference.

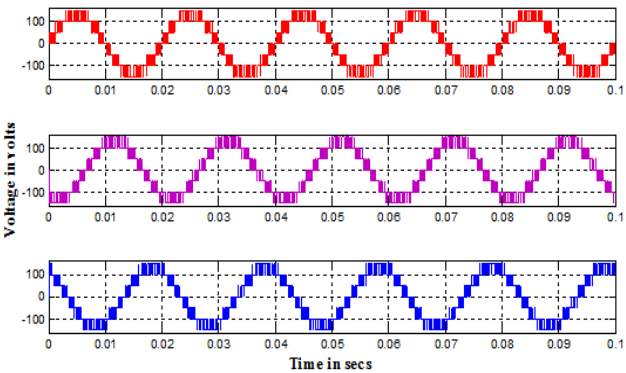

Fig. 10. Three phase output waveform for phase voltage V_P with sine reference.

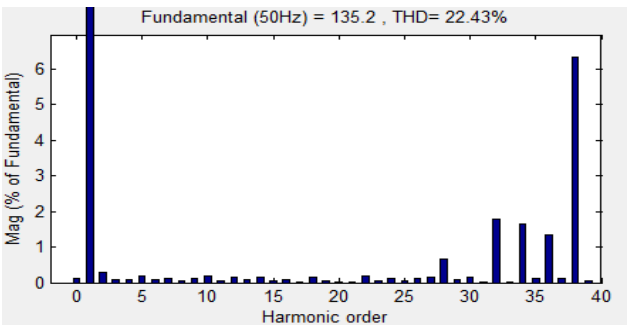

Fig. 11. FFT plot for phase voltage of BVFPWM technique with sine reference.

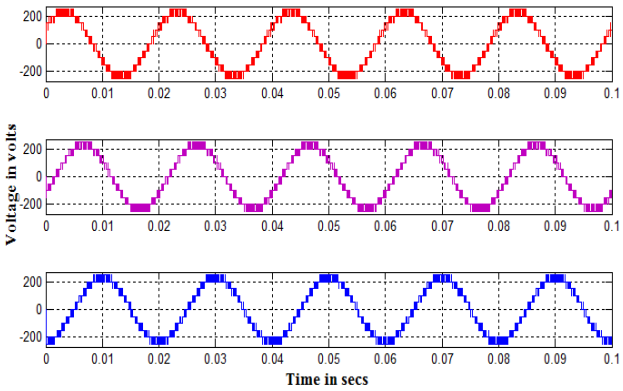

Fig. 12. Three phase output waveform for line voltage V_L with sine reference.

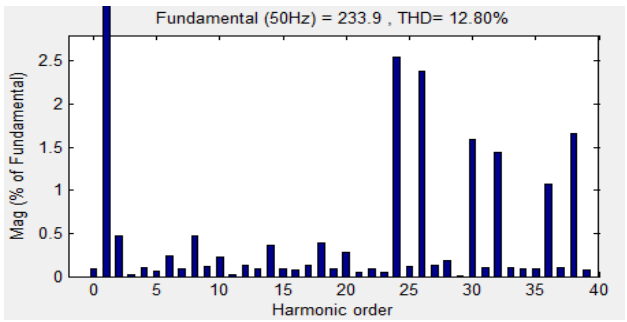

Fig. 13. FFT plot for line voltage of BVFPWM technique with sine reference.

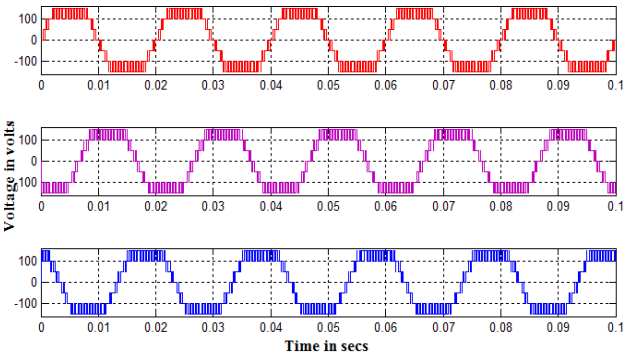

Fig. 14. Three phase output waveform for phase voltage V_P with trapezoidal reference.

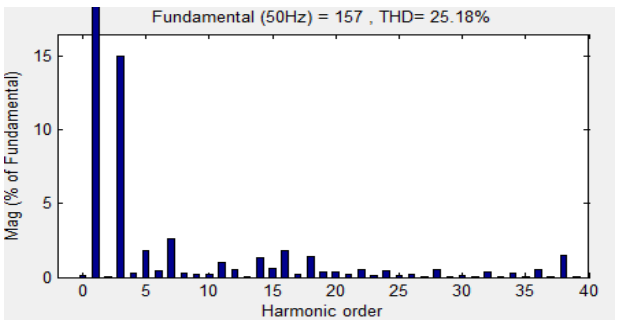

Fig. 15. FFT plot for phase voltage of BPDPWM technique with trapezoidal reference.

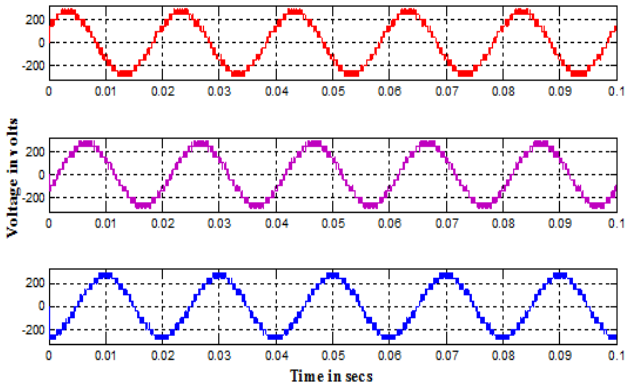

Fig. 16. Three phase output waveform for line voltage V_L with trapezoidal reference.

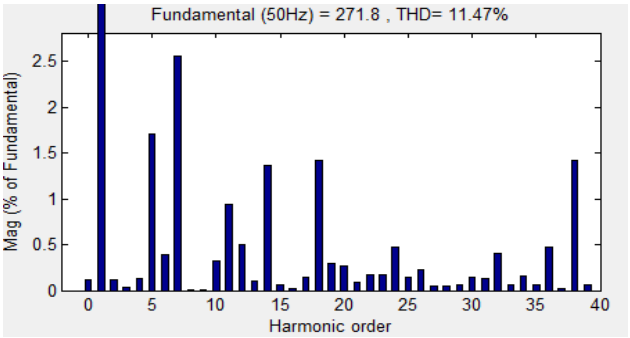

Fig. 17. FFT plot for line voltage of BPDPWM technique with sine reference.

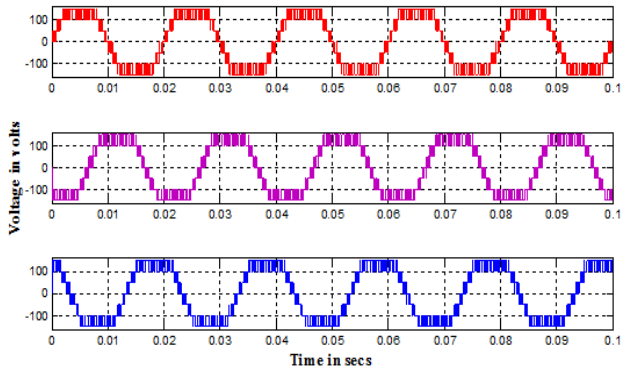

Fig. 18. Three phase output waveform for phase voltage V_P with trapezoidal reference.

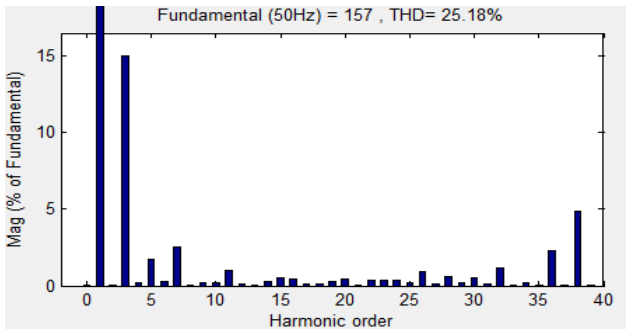

Fig. 19. FFT plot for phase voltage of BVFPWM technique with trapezoidal reference.

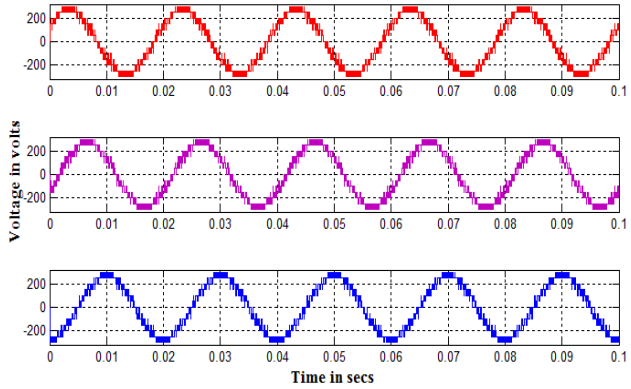

Fig. 20. Three phase output waveform for line voltage V_L with trapezoidal reference.

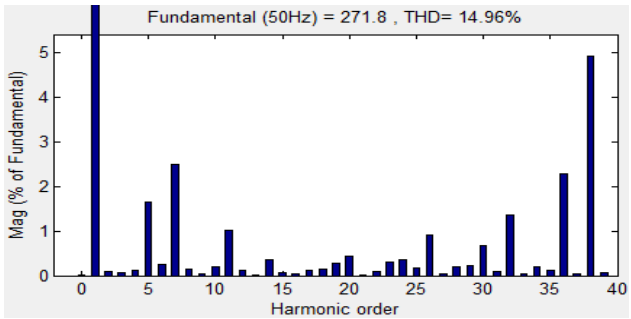

Fig. 21. FFT plot for line voltage of BPDPWM technique with sine reference.

Table 2. %THD for different modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	18.20	18.11	18.33	23.89	18.21
0.9	22.37	22.04	21.91	27.54	22.38
0.8	24.22	24	24.11	31.59	24.15
0.7	25.35	24.96	25.11	38.43	25.26

Table 3. V_{RMS} for different modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	106.1	106	106	112.7	106
0.9	95.62	95.89	95.91	104.7	95.34
0.8	84.8	84.78	84.76	95.63	84.77
0.7	74.27	74.03	74.19	84	74.22

Table 4 V_{PEAK} for different modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	259.7	259.4	259.6	159.4	149.9
0.9	233.9	233.9	234.4	148.1	134.8
0.8	207.7	207.8	207.7	135.2	119.9
0.7	182	181.7	181.9	118.8	105

Table 5. %THD for different modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	10.86	15.3	14.99	13.8	11.17
0.9	12.8	20.7	18.13	12.64	15.36
0.8	13.31	2.6	19.73	12.94	18.17
0.7	16.66	20.14	23.81	13.33	19.7

Table 6 V_{RMS} for diff modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	183.7	183.4	183.5	195.2	183.5
0.9	165.4	165.4	165.7	181.3	165.2
0.8	146.8	146.9	146.9	165.6	146.9
0.7	128.7	128.5	128.6	145.4	128.7

Table 7 V_{PEAK} for different modulation indices with sinusoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	259.7	259.4	259.6	276.1	259.5
0.9	233.9	233.9	234.4	256.4	233.7
0.8	207.7	207.8	207.7	234.2	207.7
0.7	182	181.7	181.9	205.6	182

Table 8. %THD for different modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	18.78	19.14	18.57	23.96	19.87
0.9	24.85	25.2	24.97	26.42	25.39
0.8	27.43	27.52	27.44	28.34	27.59
0.7	25.08	24.36	24.88	29.81	24.42

Table 9 V_{RMS} for diff modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	215	213.8	213.9	215.3	212.3
0.9	193.5	192.2	203.1	206	190.7
0.8	172.1	171.1	170.7	196.6	169.4
0.7	150.6	149.1	149.1	186.6	147.8

Table 10 V_{PEAK} for different modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	175.7	174.6	174.7	176	173.4
0.9	158.1	157.3	157	168.2	155.7
0.8	140.5	139.3	139.5	160.6	138.3
0.7	122.9	121.9	121.7	152.4	120.8

Table 11. %THD for different modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	9.11	10.10	10.52	12.53	10.51
0.9	11.51	19.03	14.58	12.66	13.34
0.8	12.54	21.79	20.5	12.35	14.88
0.7	13.75	17.22	16.14	11.73	14.19

Table 12. V_{RMS} for diff modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	304.1	302.4	302.4	304.5	300.2
0.9	273.7	271.8	287.2	291.3	269.7
0.8	243.3	241.8	241.4	278	239.6
0.7	213	210.8	210.8	263.9	209.1

Table 13. V_{PEAK} for different modulation indices with trapezoidal reference.

m_a	PD PWM	POD PWM	APOD PWM	CO PWM	VF PWM
1	124.2	123.4	123.5	124.5	122.6
0.9	111.8	111.2	111	118.9	110.1
0.8	99.35	98.52	98.61	113.6	97.81
0.7	86.92	86.19	86.08	107.8	85.4

6. Conclusion

As MLIs are upgrading interest, efforts are being pointed towards reducing the device count for increased number of output levels. A New MLIs is proposed in this paper to reduce the number of devices. The working principles of the proposed topology are explained and corresponding output voltages (phase voltage and line voltage) are observed. Performance factors like %THD, V_{RMS} (indicating the amount of DC bus utilization) and V_{PEAK} related to power quality issues are evaluated, presented and analyzed. Simulation carried out on a seven level inverter based on the proposed structure. Comparison of the proposed topology with conventional topologies explains that the proposed topology significantly reduces the number of power switches. The proposed topology can be effectively employed for applications where isolated DC sources are available. The advantage of the reduction in the device however, imposes two limitations: 1) requirement of isolated DC sources as is the eccentric with the CHB topology and 2) restricted modularity and fault-tolerant capabilities as compared to the Cascaded H-Bridge topology.

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