A novel design of Multilevel inverter with reduced switch topology for the integration of renewable energy sources

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Abstract–In recent days, solar energy plays a vital role in providing enormous current for the electrical appliances. Many of the industries manage their electrical issue with the solar energy. The power losses due to active devices include conduction losses and switching losses. Conduction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. But, the amount of switching harmonics is attenuated and the power loss caused by the filter inductor is reduced when filter inductor is used. Hence we proposed a new convertor having multilevel inverters which should be designed with higher voltage levels to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI). It scores good results comparing the traditional methods.

Keywords: Multilevel Inverter, H-bridge, Isolated dc-dc converter, n step, DC link.

1. Introduction

The wide use of fossil fuels gives rise to the inclusive issue of greenhouse emissions. The supplies of fossil fuels are depleted and get demand in the future. Thus, solar energy becoming more important than fossil fuels since it produces less pollution and low cost whereas the cost of fossil fuel energy is rising. The power conversion interface is significant to grating linked solar power generation systems as it converts the dc power engendered by a solar cell array into ac power and nourishes ac power into the efficacy grating. An inverter is obligatory for the power conversion interface to convert the dc power to ac power. Since the output voltage of a solar cell array is low, a dc-dc power converter is used in a small-capacity solar power generation system to boost the output voltage so that it can match the dc bus voltage of the inverter. The power conversion efficiency of the power conversion interface is imperative to ensure that there is no waste of the energy generated by the solar cell array. The active devices and passive devices in the inverter produce a power loss.

The power losses due to active devices are conduction losses and switching losses. Conduction loss is due to active devices, while the switching loss is comparative to the voltage and the current changes for each switching and switching frequency. A filter inductor is used to process the switching harmonics of an inverter and thereby the power loss is proportional to the amount of switching harmonics. The voltage change in each switching operation for a multilevel inverter is concentrated to improve its power conversion efficiency and the switching stress of the active devices. The level of switching harmonics is also attenuated, so the power loss caused by the filter inductor is also condensed. Therefore, multilevel inverter technology has been the focus of much research over the past decades. Multilevel inverters should be designed with higher voltage levels to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI).

Various voltage levels are measured by using capacitors in flying capacitor multilevel invertors and diode clamped invertors. But the power circuit is complicated it is because the implementation of asymmetric voltage expertise in both invertors and hence the increasing of voltage in multilevel inverter is unavoidable. Hence the regulation of voltage is hard in the capacitors which involved in the invertors. For instance, 12 power electronic switches are needed in diode clamped and the flying capacitor strategy for a single-phase seven-level inverter. Many kinds of innovative methods are implemented for single phase seven level inverter in decades. For instance, a seven level inverter has been introduced for photovoltaic system. It consists of six power electronic switches and three voltage levels are constructed by three dc capacitors. It ends with inconvenience in balancing the capacitor voltage. Typically, a seven level inverter possess two parts namely, level generation part and polarity generation part.

To acquire dynamic balance for the voltages of the capacitors, the modular multilevel inverter is developed which is similar to cascade H-bridge balance. The multilevel dc-link inverter overcomes the delinquent of partial shading of individual photovoltaic sources which are connected in series. The dc bus of a full-bridge inverter is arranged by numerous individual dc blocks and every dc block is constituted with a solar cell, a power electronic switch, and a diode. When the power electronics of the dc blocks is controlled, the multilevel dc-link voltages have to supply full-bridge inverter and overcome the issues of partial shading of photovoltaic sources subsequently. For attaining medium level voltage and high-power applications, many multilevel inverters has been introduced to result with wide outcome. Owing to eradicate the huge line transformers from medium voltage motor drives, five-level diode-clamped PWM inverters using 3.3-, 4.5-, or 6.5-kV insulated-gate bipolar transistors (IGBTs) is developed. But unequal identical operating conditions as long as active power flows into or out of the inverter because of four split dc capacitor. A 6.6-kV transformer-less medium-voltage motor drive using a five-level diode-clamped PWM inverter

is motivated and a three-phase diode rectifier used as the front end for energy savings of fans, blowers, and pumps without regenerative braking.

The long cable proceed as distributed parameter path in a frequency range of 100 kHz or higher. Impedance mismatch is convoyed by reflection at both inverter and motor terminals. This reflection results in high voltage at the motor terminals. When a conventional two-level inverter is used, it reaches double the inverter dc-link voltage. At the same time, five level inverter constitute with less over voltage due to the steps of the voltage are one-fourth of those of the two-level inverter. The five-level inverter has to resource the rated current with lower frequencies than the base frequency to a constant-torque load. Many of the multilevel inverter investigation is continuing to expand its capabilities, to enhance control techniques, and also to reduce both component count and manufacturing cost. Due to the limitations in voltage and to permit high-power conversion, the power switches are usually cascaded in series and organized into multilevel structures. The synthesized multilevel outputs are longer in quality which results in condensed filter supplies and size of the overall circuit. Switching losses are also constrained by using lower switching frequency operation and preserving high-power quality.

The multilevel inverter has been employed in several applications extending from medium to high power levels like motor drives, power conditioning devices also conservative or renewable energy generation and distribution. Neutral-point-clamped (NPC) or the diode-clamped inverter, cascaded multilevel, and flying capacitor (capacitor clamped) are three foremost multilevel voltage source inverters topologies. Modulation approaches exploited to multilevel inverters are selective harmonics abolition carrier-based pulse-width modulation (PWM), space vector modulation (SVM), and staircase or fundamental frequency modulation. This paper emphasizes on the cascaded multilevel inverter topology. Between the three topologies, the cascaded multilevel inverter is utmost consistent and attain the finest fault tolerance due to its modularity which is a feature that allows the inverter to continue operating at lower power levels after cell failure.

Modularity also permits the cascaded multilevel inverter to be stacked easily for high-power and high-voltage applications. The cascaded multilevel inverter comprises quite a lot of identical single-phase H-bridge cells cascaded in series at its yield margin. This is known as cascaded H-bridge (CHB) which said to be symmetrical when the dc bus voltages are equal in all the series power cells, or else considered as asymmetrical. In case of asymmetrical CHB, dc voltages are speckled to yield huge levels of output. Therefore, inverter design results with complicated circuit as every power cell has to be arranged consequently to the different power levels as well as isolated dc sources. This state creates beneficial for symmetrical CHB modularity over asymmetrical regarding maintenance and cost. In case of symmetrical cascaded inverter, the level of voltage upsurge is probable without varying dc voltage with the similar number of power cells.

In our proposed approach, five-level transistor-clamped H-bridge (TCHB) is preferred as a power call which produce five-level output in return. In contrast, it has more advantages such as huge output levels, superior quality of output, and reduction of step voltage wave fronts (DV/DT) due to motor insulation failure across the motor terminals. The compensations are great comparing to the traditional CHB approach for the very same pattern. Constant speed drive applications like fans, blowers, pumps, and compressors are more concentratedbecause these encompass 97% of currently fixed medium-voltage drives. Production plants, process industries, oil and gas sectors are some of the field where the process is utmost in handle. Multilevel inverters results a steppedoutput waveform having higher output waveform quality and lower distortion. Therefore, this inverter is applicable in wide high and medium power applications. The multilevel inverters are typically classified as three main groups,namely neutral-point clamped (NPC), flying-capacitor (FC) and the cascaded H-bridge (CHB) topologies. These conventional topologies are well reputable with their advantages and disadvantages. Cascaded multilevel inverters are constructed on aseries connection of some single-phase inverters.

The cascaded multilevel inverters can be classified as symmetrical and asymmetrical based on the consumption of the voltage. The inverter is said to be symmetric when the dc voltage sources are similar or else it is called asymmetric topology. Typically, the symmetric CHB multilevel inverters possess good modularity, butthey use a greaternumber of switches. Consequently, the asymmetric CHB multilevel inverters have been presentedto get some voltage levels for a specific number of switches. Regrettably, most of these topologies use high-voltage switches. The topologies use anH-bridge at where its switches (four switches) must be capable oftolerating the maximum operating voltage of the multilevel inverter. Unfortunately, it overthrows the concept of the multilevelinverter and result as unsuitable for medium voltage applications.

In the topology with asymmetric sources, switches have to withstand the chief ration of the maximumoperating voltage of the inverter. Conventionalmultilevel inverters have been accessible which are targeting toshrink the number of independent dc voltage sources. The proposed topologies is the modular multilevel converters (MMC) which use capacitors in its place of dc voltage sources andcontrol them using dismissed switching combinations. In contrast, atrade-off should be made between several factorsin the symmetric condition. Consequently, the proposed topology contributes exclusive flexibility in designing the multilevel inverter with respect to the purposes and limits. In the followingsection, the proposed general topology is existing, and itsmaximization by analytical equations is given. An assessment is obtained among the proposed and other topologies. The simulation and experimental results are demostrated to substantiate theproposed topology.

2. Related works

Many works related to the concepts of inverters have been illustrated. In the work of "PV permutation algorithm" [6], the inverter is controlled to remove the maximum power from each PV source under partial shading and to distribute the whole power to the load. The algorithm is constructed on a mixture of the direct pulse width modulation (PWM), the successive permutation PV sources, and the output generation to switch the multilevel dc-link inverter. The procedure is applied effectively to a seven-level inverter with distinct maximum power point tracking algorithm for each PV source and under non-uniform intensity. Digital processing unit named F28335 EZDSP is exhausted to control the PV system in the real-time mode, and MATLAB-Simulink real-time data exchange is engaged to show the extracted power and to control the system parameters by a designed graphical user interface window. Conventionally, a space vector modulation (SVM)-based approach that benefits from the switching state redundancy of an *n*-level FCC to implicitly carry out the voltage balancing task within the switching strategy [2]. Based on the voltage deviations of the capacitor voltages, a cost function is well-defined and curtailed to select the accurate redundant switching states between the available switching states. The analyses prove the competence of the proposed SVM approach to control the voltages of capacitors at their paltry reference values.

Photovoltaic Systems (PVS) can be simply assimilatedinto residential buildings later they will be the key in charge for providing low-voltage grid power flow bidirectionally [1]. Regulating issues on both the PV side and on the network side have sensed more consideration from manufacturers, rival for efficiency and low distortion and academia proposing new notions become futuristic quickly. This paper purposes at revising chunk of the topics such as MPPT, current and voltage control parting to a future paper to finish the state. Multilevel inverters are in ultra-modern power conversion schemes owing to their better-quality waveforms of voltage and current. Cascaded H-bridge (CHB) multilevel inverters have been measured as a substitute in the medium-voltage converter market and experimental electric vehicles [5]. The asymmetrical CHB (ACHB) inverter, improves the quantity of voltage levels by using dc supplies with dissimilar voltages. The CHB and ACHB inverters entail a large number of bidirectional and secluded dc supplies must be balanced. Like any multilevel inverter, they decrease the quality of power with the amplitude of voltage. This paper describes a solution to optimize the shortcomings of ACHB inverters by a high-frequency link with only one dc power source. The single power source can be nominated conferring to the application which may be regenerative, non-regenerative, and with variable or permanent voltage amplitude.

A new voltage-balancing controller for cascaded multilevel converters is presented particularly for single-phase cascaded multilevel converters [3]. It proposes a control algorithm that dedicates itself not only to balance the floating dc capacitors but also to eradicate the coupling effect between the voltage-balancing controller and the original system controller. Precisely, the average model in the d-q coordinate frame is received, and the control law is recognized. Formerly, the coupling effect between the voltage-balancing controller and the original system controller is notorious,and a new mien for adapting the duty cycle is proposed to disregard the effect. Besides, this paper bounces the design attentions of the proposed technique, with the derivation of key handover functions and effective voltage-balancing area, for the broadness of the discussion. Likewise, the reference generation systems of the voltage-balancing controller are also discussed. This paper examines the inequity in voltage in the soft-start procedure triggered by an inappropriate reference and assembles a simple modified reference generation solution. As a consequence, both simulation and experimental results authenticate the recital of the proposed control system.

An energy-balance control strategy is introduced [4] for a cascaded single-phase grid-connected H-bridge multilevel inverter linking *n* independent photovoltaic (PV) arrays to the grid. The control scheme is based on an energy-sampled data model of the PV system and enables the design of a voltage loop linear discrete controller for each array, ensuring the stability of the system for the whole range of PV array operating conditions. The control design is adapted to phase-shifted and level-shifted carrier pulse width modulations to share the control action among the cascade-connected bridges to concurrently synthesize a multilevel waveform and to keep each of the PV arrays at its maximum power operating point. Experimental results carried out on a seven-level inverter are included to validate the proposed approach.

3. Proposed method

Source is required in order to provide the energy to the circuit. It fed specific ratings of voltage and load current. The figure of circuit with power supply is depicted below. A constant low voltage controlled power supply of +5V is required for feeding input voltages to the microcontroller RS232, LM311, and LCD which need of 5 volts supply. Opto-coupler is a device which allows the transmission of a signal between parts of a circuit while keeping those two parts electrically isolated. Inside a typical Optocoupler, a LED and a phototransistor are present. When current runs over the LED, it switches on – at the point where the phototransistor senses the light and permits alternative current to flow through it. When the LED is off, current cannot flow over the phototransistor. MOSFETsare chosen due to the capability that tends to be used at frequencies less than 29 kHz. It does not have the high frequency switching capability, grip lofty currents with output greater than 5kW and have the very good thermal operating ability, being able to work properly above 100 Celsius. A multilevel inverter is a power electronic device that capable of offering expected alternating voltage level at the output terminal using multiple lower level DC voltages as an input. To generate AC voltage from the DC voltage, two –level inverter is preferred. Voltage multiplier is an

electrical circuit which is used for the conversion of AC electrical power from a lower voltage in to a higher DC voltage using a grid of capacitors and diodes. Filter is a device or process that eliminates some undesirable features from a signal. Filtering is a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal.

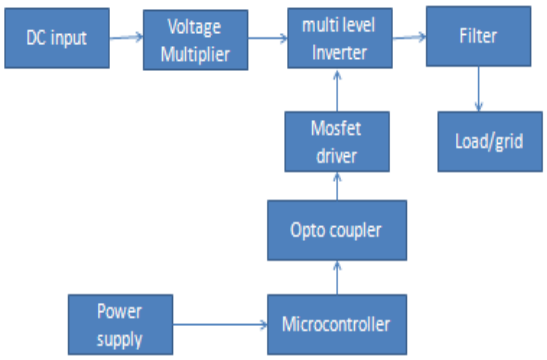

Figure 1: Block diagram

3.1. Steady-state analysis of proposed converter

The proposed converter is delivered by a low-level dc sources like battery, PV module, or fuel cell sources. It entails with a boost inductor L_s, four switches (Sm1, Sm2, Sm3, Sm4), and one *n*-stage CW voltage multiplier. Sm1(Sc1) and Sm2(Sc2) operate in a complementary mode, and the operating frequencies of Sm1 and Sc1 are defined as fsm and fsc, respectively. For suitability, modulation frequency is denoted by fsm, and alternating frequency is denoted by fsc. Hypothetically, these two frequencies should be as high as possible and smaller inductor and capacitors can be used in this circuit. In this paper, fsm is set much higher than fsc, and the output voltage is controlled by regulating the duty cycle of Sm1 and Sm2, while the output voltage current can be adjusted by fsc. As depicted in Figure, the known CW voltage multiplier is built by a cascade of periods where every period consist of two capacitors and two diodes. In an *n*-stage CW voltage multiplier, there are *N* (= 2*n*) capacitors and *N* diodes. The capacitors and diodes are alienated into odd group and even group rendering to their suffixes, as meant in Figure below.

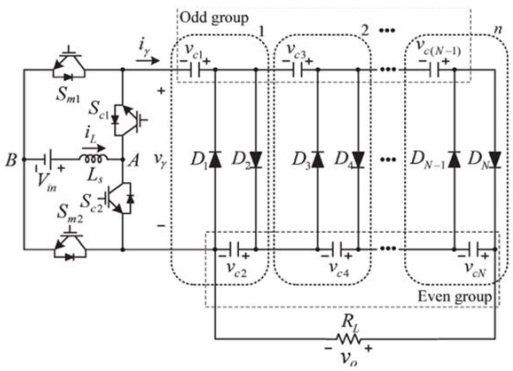

Figure 2: Steady-state analysis of proposed converter

3.2. Circuit Operation Principle

To shorten the study of circuit operation, the proposed converter with a three-stage CW voltage multiplier, as shown in Figure. 3, is used. Some assumptions are made for the further analyzation is follows.

1) Every elements of the circuit is ideal, and no power loss is found in the system.

2) When a high-frequency periodic different current is fed into the Cockcroft-Walton (CW) circuit, and every capacitors in the CW voltage multiplier are adequately bulk, the voltage drop and current of each capacitor voltage can be snubbed under a reasonable load condition. Consequently, the voltages across all capacitors are equal, except the leading capacitor whose voltage is one-half of the others.

3) The proposed converter is working in CCM and the steady-state condition.

4) When the inductor fed the storage energy to the CW circuit, any one of the diodes in the CW circuit will be conducted.

5) Several safe commutation states are overlooked. Conferring to the second assumption, each capacitor voltage in the CW voltage multiplier can be defined as

$$v_{ck} = \begin{cases} V_c/2 & for\ k = 1 \\ V_c & for\ k = 2,3,\dots,N \end{cases} \quad (1)$$

Where *vck* is the voltage of the kth capacitor and *Vc*is the steady-state voltage of *vc*2−*vcN*. For an*n*-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, which can be given by

$$V_o = nV_c \quad (2)$$

$$v_{ck} = \begin{cases} V_o/2 & for\ k = 1 \\ V_o/n & for\ k = 2,3,\dots,N \end{cases} \quad (3)$$

where V_0 is the steady-state voltage of the output load side. Figure. 3 describes the theoretical waveforms of the proposed converter, as well as switching signals, inductor current, *vγ*,*iγ*, and diode currents. Rendering to the polarity of *iγ*, the operation is divided into two parts: a positive conducting interval [$t0$, $t1$] for i_{γ_0} and negative conducting interval [*t*1, *t2*] for i_{γ_0}. During the positive conducting interval, only one of the even diodes can conduct with the sequence *D*6-*D*4-*D*2, while during the negative conducting interval, only one of the odd diodes can conduct with the sequence *D*5 −*D*3 −*D*1. Moreover, during the positive conducting interval, there are four circuit states, as shown in Fig. 4(a)–(d), denoted as states I, II-A, II-B, and II-C. In the state I, *Sm*1 turns on; thus, the energy stored in the inductor increases. In states II-A, II-B, and II-C, *Sm*2 turns on, and the inductor transfers energy to the CW circuit through *D*6, *D*4, and *D*2, respectively. Correspondingly, four circuit states are in the negative conducting interval, as shown in Figure. 4(e)–(h), denoted as states III, IV-A, IV-B, and IV-C. According to Figure. 4, the circuit operation principle of the proposed converter is illustrated in detail as follows.

1) State I: *Sm*1 and *Sc*1 are switched on, where other

switches and diodes are turned off, as shown in Figure. 4(a). The boost inductor is stimulated by the input dc source, the even group capacitors *C*6, *C*4, and *C*2 supply the load, and the odd-group capacitors *C*5, *C*3, and *C*1 are floating.

2) State II: *Sm*2 and *Sc*1 are switched on, *Sm*1 and *Sc*2 are switched off, and the current *iγ*is positive. The boost inductor and input dc source transfer energy to the CW voltage multiplier through various even diodes, as shown in Figure. 4(b)–(d). In the Figure. 4(b), state II-A, *D*6 is conducting; thus, the even-group capacitors *C*6, *C*4, and *C*2 are charged, and the odd-group capacitors *C*5, *C*3, and *C*1 are discharged by *iγ*. In Fig. 4(c), state II-B, *D*4 is conducting. Thus, *C*4 and *C*2 are charged, *C*3 and *C*1 are discharged by *iγ*, *C*6 supplies load current, and *C*5 is floating. In Fig. 4(d), state II-C, *D*2 is conducting. Thus, *C*2 is charged, *C*1 is discharged by *iγ*, *C*6, and*C*4 supply load current, and *C*5 and *C*3 are floating.

3) State III: *Sm*2 and *Sc*2 are switched on where all others are switched off, as shown in Fig. 4(e). The boost inductor is charged by the input dc source, the even group capacitors *C*6, *C*4, and *C*2 supply the load, and the odd-group capacitors *C*5, *C*3, and *C*1 are floating.

4) State IV: *Sm*1 and *Sc*2 are switched on, *Sm*2 and *Sc*1 are switched off, and the ripple *iγ* is negative. The boost inductor and input dc source transfer energy to the CW voltage multiplier through various odd diodes, as shown in Fig. 4(f)–(h). In Fig. 4(f), state IV-A, *D*5 is conducting. Accordingly, the even-group capacitors, except *C*6 which supplies load current, are discharged, and the odd-group capacitors *C*5, *C*3, and *C*1 are charged by *iγ*. In Fig. 4(g), state IV-B, *D*3 is conducting. Thus, *C*2 is discharged, *C*3 and *C*1 are charged by *iγ*, *C*6, and*C*4 supply load current, and *C*5 is floating. In Fig. 4(h), state IV-C, *D* is conducting. Thus, *C*1 is charged by *iγ*, all even capacitors supply load current, and *C*5 and *C*3 are floating.

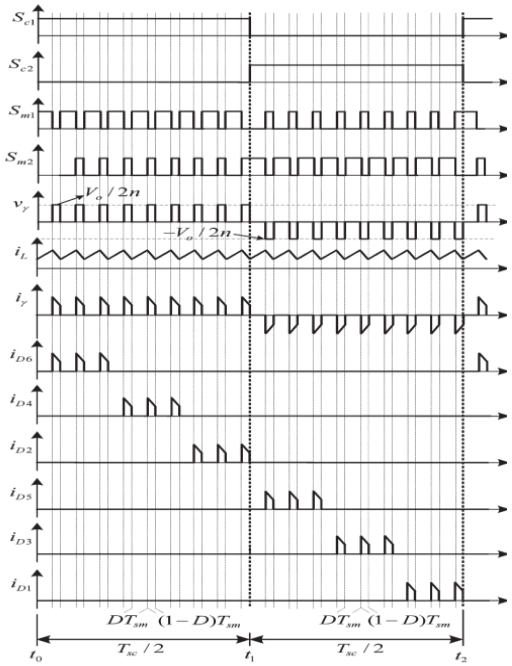

Figure 3: Theoretical waveforms of the proposed converter

3.3. Derivation of the Ideal Static Gain

From the figure shown below, it is clear that the terminal voltage of the CW circuit *V*AB = 0 in states I and III, whereas in states II and IV, *V*AB = *Vo*/2*n*. The inductor current variation, during interval 0 < *t* <*DT*sm, can be denoted by

$$\Delta i_L = \frac{V_{in}}{L_s} DT_{sm} \qquad (4)$$

Where*V*in is the input voltage, *Ls* is the boost inductor, and *D* is the duty cycle of the switch *Sm*1(*Sm*2) in the positive (negative) conducting interval through single modulation switching period *T*sm = 1/*f*sm. Then, during interval *DT*sm< *t* <(1 −*D*)*T*sm, the inductor current variation can be given by

$$\Delta i_L = \frac{V_{in} - V_o/2n}{L_s}(1-D)T_{sm} \qquad (5)$$

Beneath the steady-state condition, as per the volt-second balance principle, the voltage gain of the proposed converter can be derived from

$$M_V = \frac{V_o}{V_{in}} = \frac{2n}{1-D} \qquad (6)$$

Where $M_V$is the static voltage gain of the proposed converter. Besides, the relationship between *iγ* and *iL* can be obtained by |*iγ*|/*iL*= 1 − *D*. The connection among voltage gain and duty cycle for the proposed converter below *n* = 1−8 and the classic boost dc-dc converter is shown in Fig. 5. The proposed converter delivers high voltage gain without high duty cycle, whereas the classic boost dc-dc converter is operating at an extremely high duty cycle.

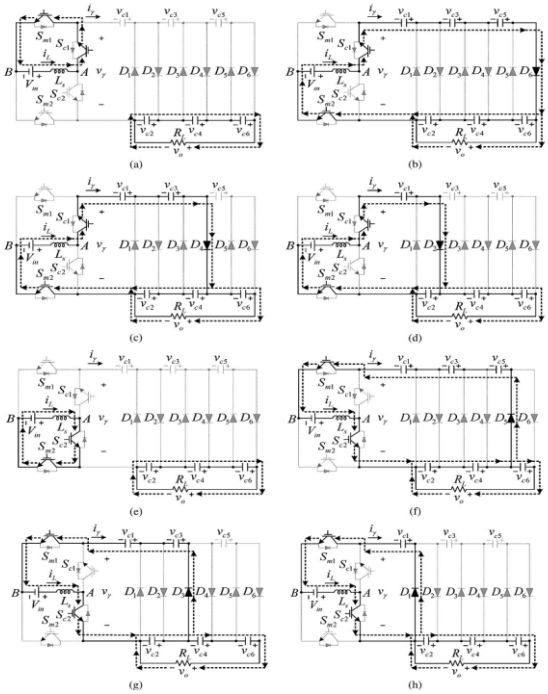

Figure 4: Circuit operation principle

3.4. The control strategy of the proposed converter

Owing to the circuit operation, the proposed converter is likely to the conventional boost dc-dc converter, but the proposed converter gives alternating current *iγ* to the CW voltage multiplier. Thus, several commercial control ICs for conventional boost converters can adapt to the proposed converter with an redundant supplementary circuit which adapts the original PWM signal to signals with appropriate timing and frequency for all the four switches.

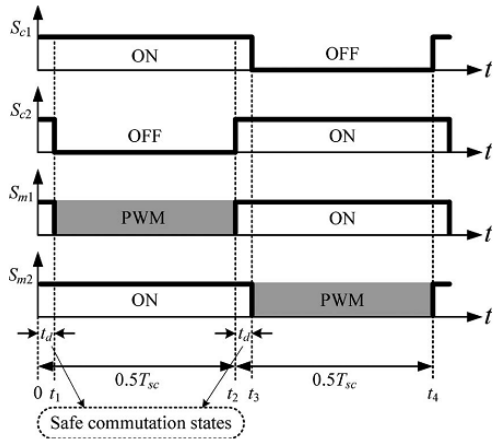

Figure 5: Timing diagram of switching patterns for the proposed converter including safe commutation states.

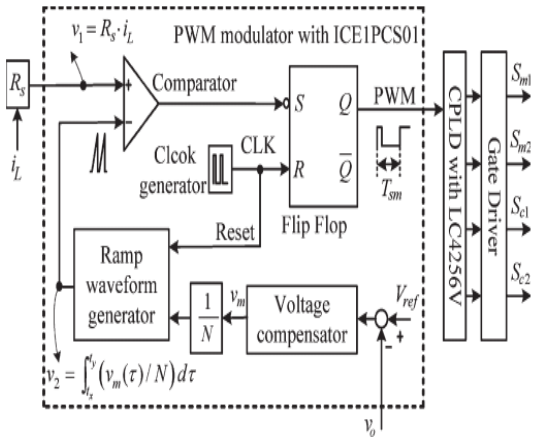

Figure 6: Control strategy of the proposed converter

Safe commutation technique is added in the control strategy of the proposed work. Having a glimpse at the figure deeply, it is clear that *Sc*1 and *Sc*2 (*Sm*1 and *Sm*2) swap the conduction states at the altering instant among each state. When the commutation be unsuccessful, the intermittent inductor current will found a voltage spike and affect the switching elements. In the switching approach, four switches of the proposed converter is not comprising safe commutation technique. In contrast, alternative switching strategy including safe commutation technique under the similar output function, is depicted in Figure 6.This switching method is implemented in the control strategy of the proposed converter to prevent open circuit of the inductor. The switching outlines of *Sc*1 and *Sc*2 residence a small overlap time, whereas *Sm*2 (*Sm*1) preserves a high trigger level if *Sc*1 (*Sc*2) is switched on; It provides a safe commutation to the operation of the proposed converter. In this paper, an average-current mode control will be used to design the PWM modulator to realize the proposed converter in CCM. In order to enabling the design, this paper organizes CE1PCS01 as the main controller for the PWM modulator, and it approves the quasi-steady-state approach by consuming one cycle control method on leading-edge modulation, as revealed in Figure. 6, in which, the protective control devices are gone[7]. In case of quasi-steady-state approach [8], theobjective oof controlling is to offer a resistor emulator, assembling the input current $i_L$to be proportional to the input voltage V_{in}. The emulated resistance $R_e$is given by

$$R_e = \frac{V_{in}}{\langle i_L \rangle} \quad (7)$$

where i_L is the average of the input current through one modulation period T_{sm}. Substituting (6) into (7), the emulated resistance can be altered as

$$R_e = \frac{V_o \cdot (1-D)}{N \cdot \langle i_L \rangle} \quad (8)$$

Where*N* = 2*n*. Typically, *Re* can be controlled by the subsequent control law [9]:

$$R_s \cdot \langle i_L \rangle = \frac{v_m}{M_V} \quad (9)$$

Where*Rs*is defined as the equivalent current-sensing resistance, and v_m is the modulation voltage, which is resolute by the error command among the reference values v_{ref} and actual valuev_0, as presented in Figure 6. The voltage compensator is sourced to control the output voltage $v_0$over $v_m$to supply appropriate power to the load. Replacing (8) in to (9)

$$R_e \cdot \langle i_L \rangle = \frac{V_o \cdot (1-D)}{N} (10)$$

Bestowing to (8) and (10), *Re* can be characterized as

$$R_e = \frac{R_s \cdot V_o}{v_m} (11)$$

It is obvious from the equation (11), that when the modulation voltage $v_m$is organized to be a constant, the emulated resistance $R_e$will be a constant. As a result, the input current will be directly proportional to the input voltage as described in equation (7). Alternatively, the proposed converter operating in CCM can be accomplished and relaible. The enactment of this concert has to control the duty cycle *D* of the PWM modulator to fulfill the control law (10). From the figure 6, One-cycle control technology is utilized on leading edge modulation, the PWM modulator is assembled by a constant time clock generator, a voltage comparator, an SR flip-flop, and a ramp waveform generator with a reset. In case of practical applications, the average inductor current have the chances to be approximately equal to the instant inductor when the current ripple in the inductor is negligible during one

modulation period [9]. Therefore, in this paper, the functions *v*1 and *v*2, are set to implement the control law (10). The PWM signal including boost function in CM is obtained from the operation of the PWM modulator. The PWM signal is fed into a preprogrammed complex programmable logic device, CPLD LC4256V, as shown in Fig. 6. A timer established in the CPLD is used to set the alternating period T_{sc} or alternating frequency f_{sc} . Additionally, a logical circuit programmed in the same CPLD varies the PWM signal from the microcontroller (ICE1PCS01) and sends the modified signals in order to trig the four switches. An overlap with interval *td* for safe commutation is implemented in the CPLD as well.

4. Results and discussion

A three-phase, 415-V, 7.5-KW, 50-Hz induction motor (IM) is driven with the nine-level inverter using open-loop V/f control scheme.

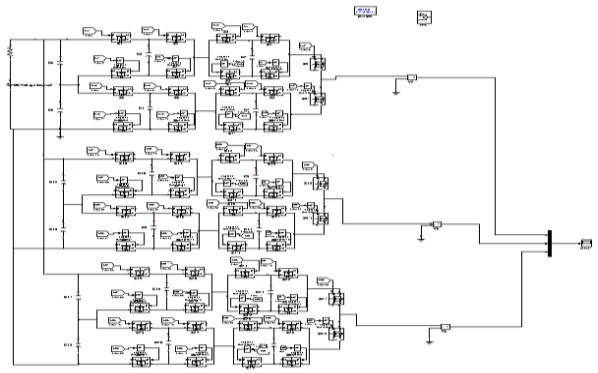

Figure 7: Simulation diagram for nine level inverter by stacking multi-level converters.

Here, the H Bridge is made common to both the FC and the selector switches are connected in between. Here, the H-bridge switches need to switch throughout the cycle.

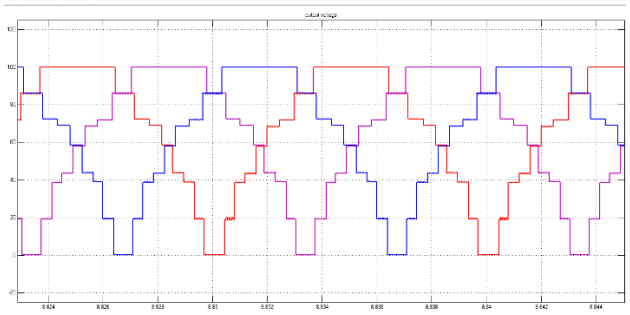

Figure 8: Nine-level output voltage.

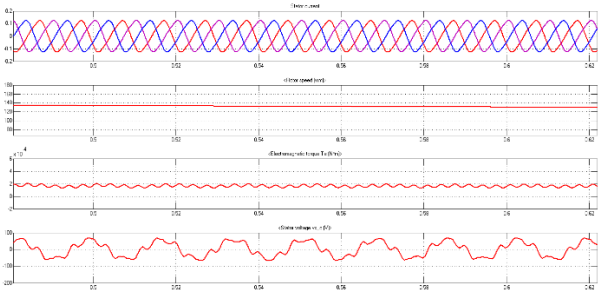

Figure 9: The motor parameter of stator current, rotor speed, torque and stator voltage.

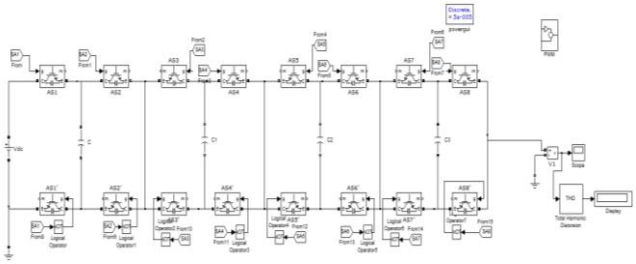

Figure 10: The simulation diagram for the proposed inverter.

It is hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges.

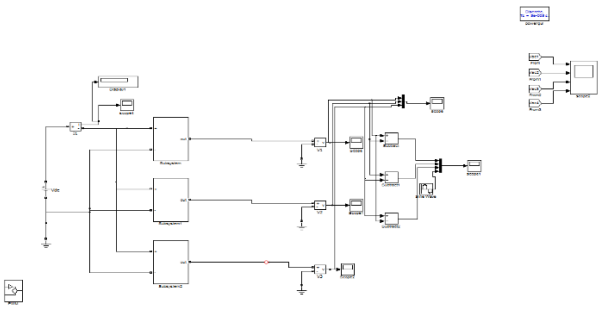

Figure 11: The simulation diagram of 3 phase inverter.

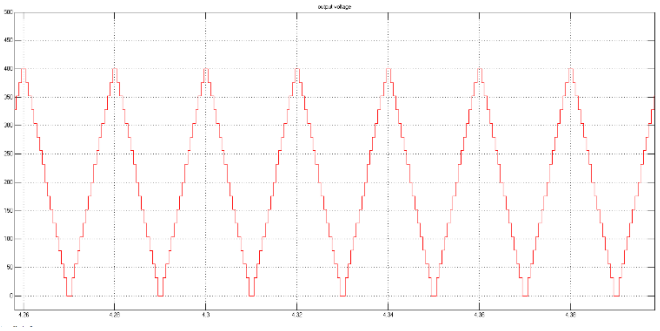

Figure 12: seventeen-level output voltage for the proposed inverter.

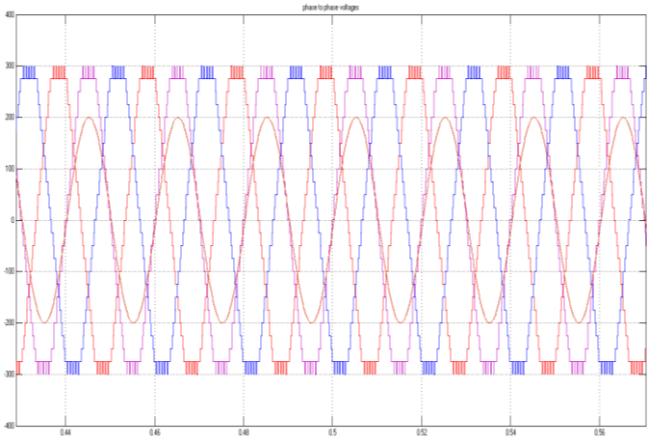

Figure 13: Phase to phase output voltage.

Parameter	Existing System	Proposed System
No. Of Switches	18	16
No. Of Sources	2	1
Output Levels	9	17
Topology	Stacked Multilevel Inverter (Flying Capacitor + H Bridge)	Flying Capacitor + floating capacitor H-Bridge
Algorithm	Hysteresis Based Capacitor voltage balancing algorithm	Space vector control algorithm

Table 1: Comparison between existing and proposed system

5. Conclusion

The proposed converter affords the gain with high voltage without any maximum high duty cycle when in contrast to traditional methods. The proposed work has reduced number of sources, switches with high output levels (seventeen-level). In this work, Flying Capacitor and floating capacitor H-Bridge is used which operated Space vector control algorithm. The measured output voltage of phase for every cell and the phase-to-phase voltage, suggesting uniform power distribution among the cells. As a consequence, in the line voltage, 17 level inverter voltage were produced and thus guarantees for high output quality.

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