NEUTRAL POINT POTENTIAL BALANCING ALGORITHM FOR SLIDING MODE CONTROLLED THREE-LEVEL ACTIVE POWER FILTER

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Abstract: *In this paper, the authors present a study of the instability problem of the input DC voltages of the three-level Neutral Point Clamping (NPC) Active Power Filter (APF). This APF is applied for the enhancement of voltage network power quality by compensation of harmonic currents produced by a nonlinear load. In the first part, the authors present a topology of three-level NPC Voltage Source Inverter (VSI), and its space vector diagram. In the second part, as solution for instability problem of the input DC voltages of the APF, the authors propose a simplified Space Vector Pulse Width Modulation (SVPWM) with neutral point potential control. After that, the sliding mode regulator used to control the APF is developed. Stable DC bus supply associated with sliding regulator of APF allows getting low harmonic content network currents with unity power factor.*

Key words: *Active power filter, NPC multilevel inverter, space vector pulse width modulation (SVPWM), Neutral point potential control, nonlinear load.*

1. Introduction

The widespread use of power electronics in domestic and industrial application had induced power line losses and electrical interference problems, which resulted in low power factor, efficiency and bad quality of the power electrical distribution system.

Classical solutions use passive filters, made up of capacitors and inductors, to reduce line current harmonics and to compensate reactive power. But these filters have several drawbacks: risk of parallel and series resonance with the AC source, bulky passive components, and low flexibility due to fixed compensation characteristics.

An alternative solution is to use active power filters, especially the shunt filter, which is the most suitable for harmonic current elimination and reactive power compensation [1].

The structures of the filters knew an evolution, from two-level converters [2,3] to multilevel converters [4-6]. Various topologies are developed such as flying capacitor multilevel converters, diode clamped multilevel converters, NPC multilevel converters, and H bridge multilevel converters.

The unbalance of the different DC voltage sources of the three-level (NPC) active power filters constitutes the major limitation for the use of these power converters.

Several methods are proposed to suppress the unbalance of neutral point potential, generally using redundant vectors. Some of these methods are based on adding a zero sequence or a dc-offset to output voltage [7,8]. In [9,10], power electronics circuitry is added to redistribute charges between capacitors. A method based on minimizing a quadratic parameter that depends on capacitor voltages is presented in [11]. This quadratic parameter is positively defined and reach zero when the two capacitors have the same voltage. Some other works use a converter-inverter cascade [12], and apply automatic control methods, such as fuzzy logic control [13] or sliding mode control [14] to this cascade. The drawback of these methods is either high costs and system complexity, or the use of open loop scheme. In this work we use a simple and closed loop method which makes a continuous measurement of output current and difference between capacitors voltages, and choose the redundant vector on the basis of these measurements.

In this paper, first part is dedicated to the presentation of the model of the three phases three-level NPC VSI with its space vector diagram. In the second part, the simplified SVPWM algorithm with the proposed neutral point potential control algorithm are presented. This APF is applied for the enhancement of voltage network power quality by compensation of harmonic currents produced by a nonlinear load (Fig. 1). At the end the simulation results of sliding mode controlled APF are presented.

Fig. 1. Synoptic diagram of application of shunt APF on power supply fed nonlinear load

2. Modelling of three-level NPC voltage source inverter

The three phases three-level NPC VSI is constituted by three legs and two DC voltage sources. Each leg has four bi-directional switches in series, and two diodes to get the zero voltage for V_{KM} (Fig. 2). Each switch is composed by a transistor and a diode in anti-parallel [15].

The switch connection function F_{KS} indicates the opened or closed state of the switch T_{KS}:

$$F_{KS} = \begin{cases} 1 & \text{if } T_{KS} \text{ close} \\ 0 & \text{if } T_{KS} \text{ open} \end{cases} \quad (1)$$

For a leg K of the three phases three-level NPC VSI, several complementary control laws are possible. The optimal control law of this inverter is:

Fig. 2. Three-level NPC voltage source inverter

$$\begin{cases} F_{K4} = 1 - F_{K1} \\ F_{K3} = 1 - F_{K2} \end{cases} \quad (2)$$

Half leg connection function F_{Km}^b is defined as:

$$\begin{cases} F_{K1}^b = F_{K1} F_{K2} \\ F_{K0}^b = F_{K3} F_{K4} \end{cases} \quad (3)$$

m =1: for the lower half leg;
m =0: for the upper half leg.

As indicated in Table 1, each leg of the inverter can have three possible switching states, P, O, or N. When the top two switches T_{i1} and T_{i2} are turned on, the switching state is P. When the medium switches T_{i2} and T_{i3} are turned on switching state is O. When the lower switches T_{i3} and T_{i4} are turned on, the switching state is N.

Fig. 3 shows the space vector diagram for three-level inverter. Since three kinds of switching states exist in each leg, this converter has 27 switching states, as indicated in the diagram. The output voltage vector can take only 18 discrete positions in the diagram because some switches state are redundant and create the same space vector.

Fig. 3. Space vector diagram of a three-level inverter

3. Three-level inverter control

a. Space vector modulation for two-level inverter

Fig. 4 shows structure of two-level inverter. Each one of the three phases of the inverter has two switches and two freewheeling diodes. Depending on the values of the switching signals, the two-level inverter has eight states, summarized in Table 2, where it is also indicated the output voltage vector produced in each state. These output vectors are shown on the space vector diagram of Fig. 5. It is also indicated an arbitrary reference vector V^*, to be generated by the inverter.

The desired voltage vector, V^*, located in a given sector, can be generated by a linear combination of the two adjacent base vectors, v_x and v_y, which are framing the sector, and one of the two zero vectors v_z.

$$V^* = d_x v_x + d_y v_y + d_z v_z \quad (4)$$

Table 1
States of three-level inverter

Switching Symbols	Switching States				Output Voltage
	T_{i1}	T_{i2}	T_{i3}	T_{i4}	
P	ON	ON	OFF	OFF	U_{c1}
O	ON	OFF	ON	OFF	0
N	OFF	OFF	ON	ON	$-U_{c2}$
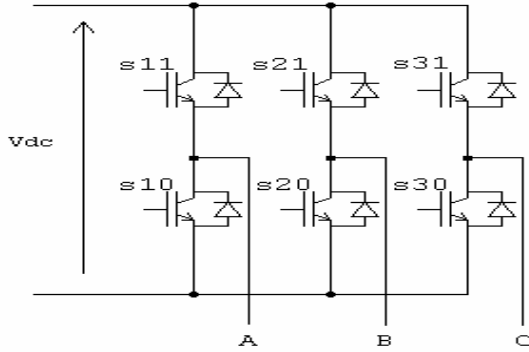
Fig. 4. Two-level inverter structure

Table 2
States of two-level inverter

State	F_a	F_b	F_c	Voltage vector
0	0	0	0	V_0
1	0	0	1	V_1
2	0	1	0	V_2
3	0	1	1	V_3
4	1	0	0	V_4
5	1	0	1	V_5
6	1	1	0	V_6
7	1	1	1	V_7

d_x, d_y and d_z denotes the so called duty ratios of states X, Y and Z of the inverter within the switching interval, respectively.

The duty ratios d_x, d_y and d_z are calculated as [16,17]:

$$d_x = \frac{\left|V^{2*}\right|}{\sqrt{2/3}V_{dc}} \frac{\sin(60-\theta)}{\sin(60)}$$

$$d_y = \frac{\left|V^{2*}\right|}{\sqrt{2/3}V_{dc}} \frac{\sin(\theta)}{\sin(60)} \qquad (5)$$

$$d_z = 1 - d_x - d_y$$

b. Simplified SVPWM for three-level inverter

In this work, we present a simple and fast method that divides the space vector diagram of three-level inverter into six small hexagons. Each hexagon is space vector diagram of two-level inverter, as shown in Fig. 6.
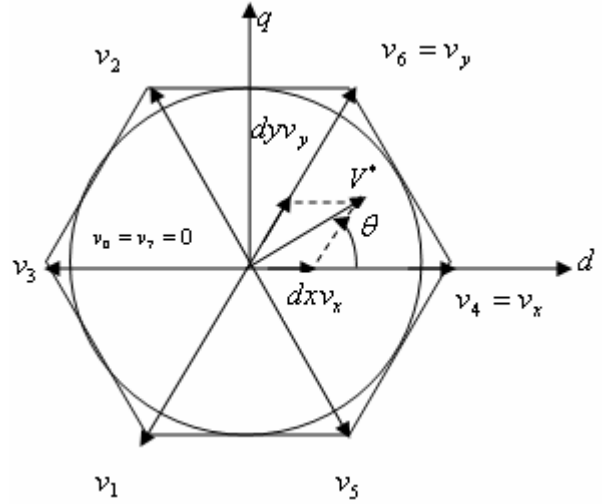
Fig. 5. Space vector diagram of two-level inverter
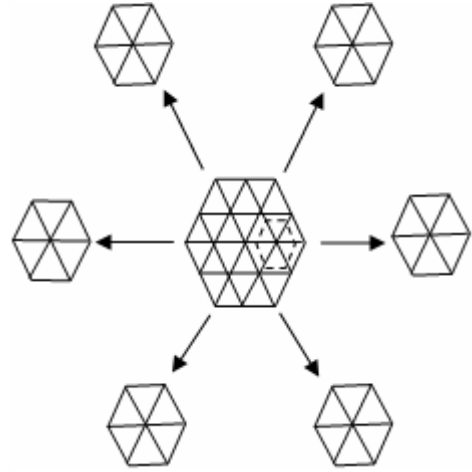
Fig. 6. Decomposition of space vector diagram of a three-level inverter to six hexagons
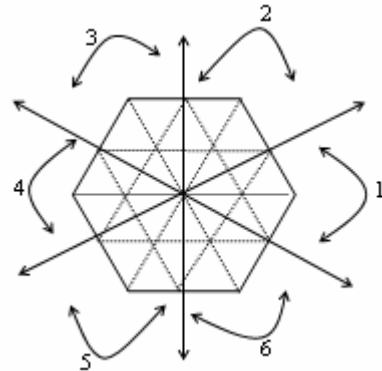
Fig. 7. Division of overlapped regions

To reach this simplification, two steps have to be done. Firstly, from the location of the given reference voltage, one hexagon has to be selected among the six small hexagon of the three-level space vector diagram.

There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons as shown in Fig. 7. Each hexagon is identified by a number S defined in equation (6). Secondly, we translate the origin of the reference voltage vector towards the center of the selected hexagon as indicated in Fig. 8. This translation is done by subtracting the center vector of selected hexagon from the original reference vector. Table 3 gives the components d and q of the reference voltage V^{2*} after translation, for all the six hexagons. The index (^{2}) or (^{3}) above the components indicate two or three-level cases respectively.

$$s = \begin{cases} 1 & if \quad -\pi/6 < \theta < \pi/6 \\ 2 & if \quad \pi/6 < \theta < \pi/2 \\ 3 & if \quad \pi/2 < \theta < 5\pi/6 \\ 4 & if \quad 5\pi/6 < \theta < 7\pi/6 \\ 5 & if \quad 7\pi/6 < \theta < 3\pi/2 \\ 6 & if \quad 3\pi/2 < \theta < 11\pi/6 \end{cases} \quad (6)$$
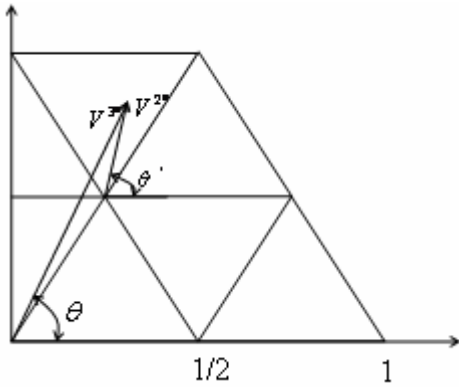
Fig. 8. Translation of reference voltage vector

Table 3
Correction of reference voltage vector

s	v_d^{2*}	v_q^{2*}
1	$v_d^{3*} - 1/2$	v_q^{3*}
2	$v_d^{3*} - 1/4$	$v_q^{3*} - \sqrt{3}/4$
3	$v_d^{3*} + 1/4$	$v_q^{3*} - \sqrt{3}/4$
4	$v_d^{3*} - 1/2$	v_q^{3*}
5	$v_d^{3*} + 1/4$	$v_q^{3*} + \sqrt{3}/4$
6	$v_d^{3*} - 1/4$	$v_q^{3*} + \sqrt{3}/4$

C. Neutral Point potential control method

In the space vector diagram of three-level inverter (Fig. 3), we can distinguish four types of vectors: large vectors, medium vectors, small vectors and zero vectors. The large vectors are the vectors that all of three legs are connected to either point P or N, except in the case of all the three being connected at the same point. There are six large vectors in the space vector diagram: PNN, PPN, NPN, NPP, NNP and PNP. The medium vectors are the ones that only one phase is connected to point O and other two phases are connected to P and N each other. There are six medium vectors: PON, OPN, NPO, NOP, ONP and PNO. The small vectors are those vectors that have two phases connected at the same point. There are twelve of them: PPO, OON, OPO, NON, OPP, NOO, OOP, NNO, POP, ONO, POO and ONN. The zero vectors are the vectors that have all three phases are connected at the same point. There are three zero vectors: PPP, OOO and NNN.

To show the effect of each type of vectors on the neutral point potential, we present the load connections of one example of each type in Fig. 9. It may be easily deduced from Fig. 9.a and Fig. 9.d that neither zero vectors nor large vectors inject current in the neutral point O. So they do not change the voltage of neutral point.

Fig. 9.b shows that medium vectors can inject current in the neutral point. Fig. 9.c1 and Fig. 9.c2 show two small vectors with two different switching combinations: POO and ONN. These two vectors product the same output voltage, but when the vector POO is applied, the current flows into the neutral point ($I_{d0} = -i_1$), while with the vector ONN, the current flows out ($I_{d0} = i_1$)(Fig.2).

Table 4 shows the current injected by all small and medium vectors [18]. As we see, each small redundant vector can inject either positive or negative current. Those small vectors injecting positive phase currents into the neutral point will be called positive vectors (ONN, PPO, NON, OPP, NNO, POP), while those injecting opposite phase currents will be called negatives vectors (POO, OON, OPO, NOO, OOP, ONO).

Medium vectors also affect neutral point potential. However, as they are not redundant vectors, this influence will not be controlled, being therefore considered as perturbation for the dc-voltage stabilization [19,9]

The neutral point potential control is based on the use of both two redundant vectors in each sector, in order to inject positive or negative current in neutral point, depending on the value of the two capacitors voltages and the load current (7).

$$c\frac{dU_{c1}}{dt} = I_{red} - I_{d1}$$
$$c\frac{dU_{c2}}{dt} = I_{red} + I_{d2}$$
$$I_{d0} = -(I_{d1} + I_{d2}) \quad (7)$$
$$I_{d1} = F11 \cdot F12 \cdot i_1 + F21 \cdot F22 \cdot i_2 + F31 \cdot F32 \cdot i_3$$
$$I_{d2} = F13 \cdot F14 \cdot i_1 + F23 \cdot F24 \cdot i_2 + F33 \cdot F34 \cdot i_3$$
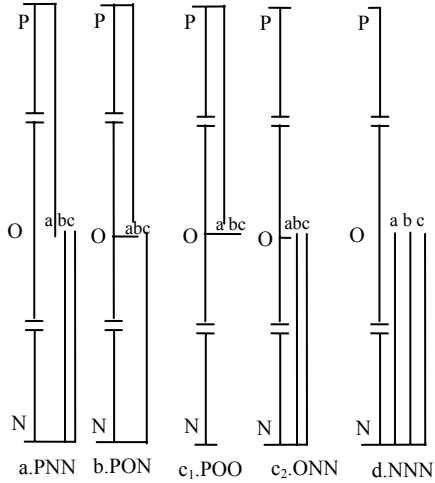
Fig. 9. Neutral point connections

Table 5 shows the current injected by the six small vectors. By using this table, one proposes the neutral point potential control algorithm of this converter as indicated by (8) (9) (10).

Table 4
Neutral point current of different space vectors

Positive Small vectors	I_{d0}	Negative Small vectors	I_{d0}	Medium Vectors	I_{d0}
ONN	i_1	POO	$-i_1$	PON	i_2
PPO	i_3	OON	$-i_3$	OPN	i_1
NON	i_2	OPO	$-i_2$	NPO	i_3
OPP	i_1	NOO	$-i_1$	NOP	i_2
NNO	i_3	OOP	$-i_3$	ONP	i_1
POP	i_2	ONO	$-i_2$	PNO	i_3

Table 5
Neutral point current of small space vectors

Vectors	Redundancy (a)	I_{d0}	Redundancy (b)	I_{d0}
Vector 1	ONN	i_1	POO	$-i_1$
Vector 2	PPO	i_3	OON	$-i_3$
Vector 3	NON	i_2	OPO	$-i_2$
Vector 4	OPP	i_1	NOO	$-i_1$
Vector 5	NNO	i_3	OOP	$-i_3$
Vector 6	POP	i_2	ONO	$-i_2$

For vector 1 and vector 4

$$\begin{cases} if & U_{c1} \geq U_{c2} & \& & i_1 \geq 0 & \Rightarrow \text{redundancy (b)} \\ if & U_{c1} \geq U_{c2} & \& & i_1 \leq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_1 \geq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_1 \leq 0 & \Rightarrow \text{redundancy (b)} \end{cases} \quad (8)$$

For vector 2 and vector 5

$$\begin{cases} if & U_{c1} \geq U_{c2} & \& & i_3 \geq 0 & \Rightarrow \text{redundancy (b)} \\ if & U_{c1} \geq U_{c2} & \& & i_3 \leq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_3 \geq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_3 \leq 0 & \Rightarrow \text{redundancy (b)} \end{cases} \quad (9)$$

For vector 3 and vector 6

$$\begin{cases} if & U_{c1} \geq U_{c2} & \& & i_2 \geq 0 & \Rightarrow \text{redundancy (b)} \\ if & U_{c1} \geq U_{c2} & \& & i_2 \leq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_2 \geq 0 & \Rightarrow \text{redundancy (a)} \\ if & U_{c1} \leq U_{c2} & \& & i_2 \leq 0 & \Rightarrow \text{redundancy (b)} \end{cases} \quad (10)$$

4. Active Power Filter Control

A voltage source of 220V, 50Hz feeds a three phases nonlinear load illustrated in Fig. 1. This load produces distorted phases currents with THD of respectively 120%, 104 % and 76% which is above the tolerated THD limit standard. These currents with their spectral analysis are presented in Fig. 10.

Active power filter is controlled using sliding mode regulator [20,21]. From the model of active filter associated to supply network (11) and by considering the error between harmonic current reference and the active filter current as sliding surface (12), and the smooth continuous function as attractive control function (13), one gets the control law (14).

$$V_{frefK} - V_K = R_f i_{fK} + L_f \frac{di_{fK}}{dt} \quad (11)$$

with : $V_K = V_{SK} - R_s i_{SK} - L_s \frac{di_{SK}}{dt}$;
K = 1,2 and 3

$$S_s = i_{frefK} - i_{fK} \quad (12)$$

$$U_n = k.\frac{S_s}{|S_s| + \lambda} \quad (13)$$

$$V_{frefK} = R_f i_{fK} + L_f \frac{di_{frefK}}{dt} + V_K + k\frac{S_s}{|S_s| + \lambda} \quad (14)$$

Fig. 11 shows the DC bus capacitors voltages of three-level APF. We can note that the capacitors voltages difference increases continuously. The application of SVPWM with neutral point potential control at t =1,3s pushes these voltages toward the reference of E/2 keeping them equal.

Instantaneous real and imaginary powers method is used to identify reference harmonic currents. Its algorithm is presented in Fig. 12.

Reference identified harmonic current i_{fref1} and output filter current i_{f1} are almost superimposed as presented in Fig. 13.

Fig. 14.a,b,c presents main source voltages and currents after harmonic currents compensation. Spectral analysis of each current is illustrated in Fig. 14.d,e,f. It is shown that source currents are

almost sinusoidal with THD of respectively 1.9%, 2.4% and 2.3% and unity power factor.
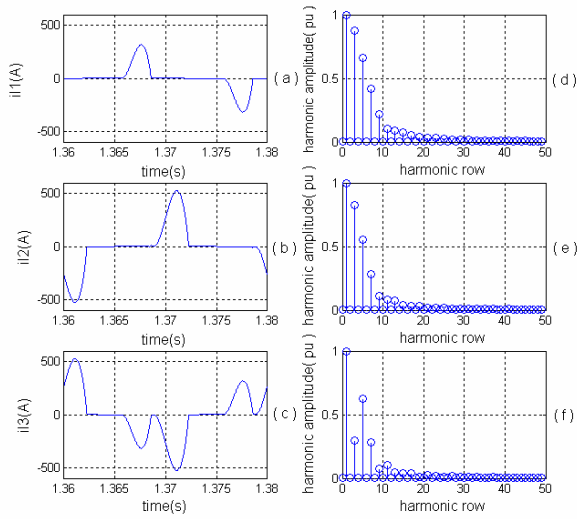
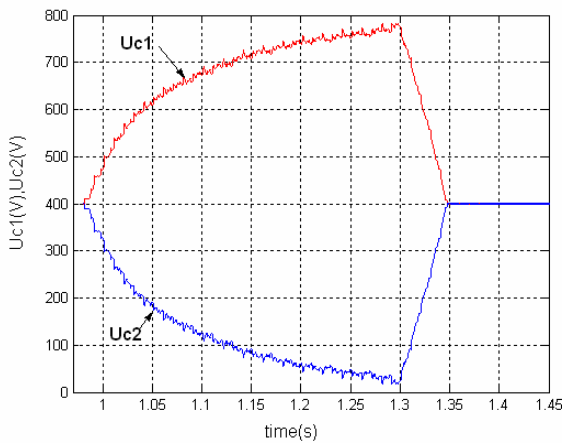

Fig. 10. Load currents

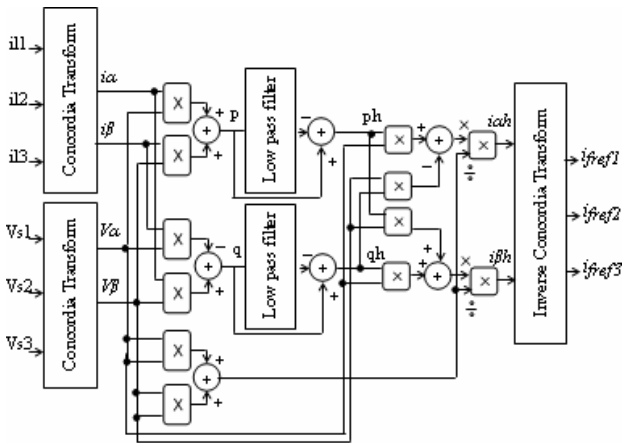Fig. 11. DC bus condensers voltages of three-level APF

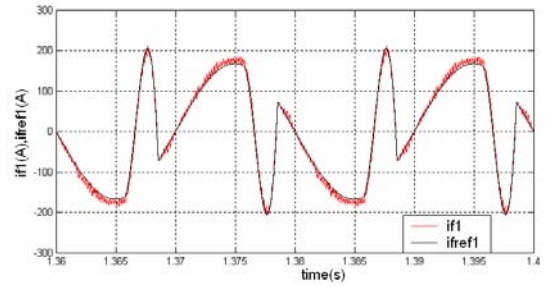Fig. 12. Instantaneous real and imaginary powers harmonic current identification algorithm

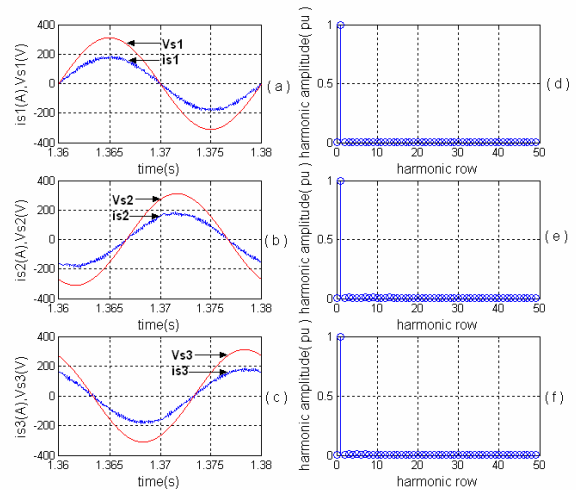Fig. 13. Reference harmonic current i_{fref1} and filter output current i_{f1}

Fig. 14. Main source voltages and currents with their spectral analysis

5. Conclusion

In this paper, one studies the problem of unbalanced input capacitors DC voltages of three-level NPC shunt active power filter.

The study of the instability problem of the input DC voltages of this converter shows that its different input voltages are not stable, which implies a bad harmonic current compensation.

To solve this instability problem, one proposes to use a simple and closed loop method which makes a continuous measurement of output current and difference between capacitors voltages, and choose the redundant vector on the basis of these measurements.

The application of the proposed simplified SVPWM with neutral point potential control makes the input DC link voltages stable.

Stable DC bus supply of sliding mode controlled three-level NPC shunt APF allows getting balanced main source currents with low total harmonic distortion and unity power factor.

The results obtained in this work show that the proposed solution allows using this topology to compensate the harmonic current and reactive power in high power utilities.

6. Appendix

Main source:
$V_{ph\text{-}ph}$= 380V, f=50Hz, R_s = 0.0001Ω, L_s = 0.0001H.
Active power filter:
E = 800V, R_f = 0.001Ω, L_f = 0.0005H, C=0.005F, f_c=5kHz.
Nonlinear load
R1=20Ω, R2=10 Ω, C1=0.05F, C2=0.05F.

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