SWITCHING FREQUENCY EFFECTS AND EFFICIENCY ANALYSIS OF QUADRATIC BUCK CONVERTER FOR LOW OUTPUT VOLTAGE AND HIGH CURRENT APPLICATIONS

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Abstract: *A well known feature of the Quadratic Buck Converter (QBC) is its voltage conversion ratio which has a quadratic dependence on the duty cycle. As in most dc-dc converters, when the switching frequency of QBC is increased, it results in improving the dynamic response besides reducing the size and cost of reactive components. However, it has a downside. The higher switching frequency leads to a system efficiency degradation and greater power dissipation. This paper will throw light on switching frequency selection and efficiency analysis of the QBC in case of low output voltage and high current applications. A small-signal modeling of the QBC is presented here using state-space averaging technique. The QBC is implemented with digital average current-mode (ACM) control strategy and the simulation results are presented using PSIM software. The switching frequency selection and efficiency analysis are carried out using MATLAB software to obtain the performance characteristics of the QBC. Hence, the need for a trade-off between converter efficiency and transient response.*

Key words: *Quadratic buck converter (QBC), voltage-mode (VM), average current-mode (ACM), transient settling time (TST), transient voltage deviation (TVD), steady state voltage ripple (SSVR), synchronous rectification (SR).*

1. Introduction

Switched mode dc-dc converters are widely used as power processors in modern electronic equipment owing to their compactness, low weight and higher energy efficiency. Laptop computers [1], [2] use advanced microprocessors, which operate at very high clock frequencies (GHz) while computing complex algorithms. This results in more power consumption which is proportional to clock frequency and square of the CPU core voltage. In order to minimize power consumption, the microprocessors are fed with very low voltage (around 1V). This paper gives a focus on the duty cycle extended quadratic buck converter (QBC) in order to achieve tight and accurate voltage regulation. Generally, the source to power the laptop is either a battery or an AC adapter. The existing non-isolated dc-dc converters like buck, multi-phase non-coupled and coupled buck [3-12] are unsuitable for large input voltage reduction (19V-1V) because of minimum turn-on time requirement of the switch. This constraint limits their operation to lower switching frequencies. The other major problems associated with buck converter are drop-out voltage, loss of current limit, and also synchronous rectification (SR) implementation. These problems collectively enhance the conduction losses at higher conversion ratios. The above said limitations can be overcome by the QBC [13-19] as its dc conversion ratio has a quadratic dependence on the duty cycle. A large output voltage swing can be obtained for small variations in the duty cycle as compared to the buck converter.

In case of quadratic buck converter, that is operating in continuous conduction mode (CCM), the control-to-output voltage transfer function has two complex right-half-plane (RHP) zeros [20]. These RHP zeros will limit the control bandwidth and as a result of which the dynamic performance of the converter becomes sluggish. In the technical literature surveyed, many control strategies have been proposed and analyzed. Among them, the most popular are voltage-mode (VM) and the average current-mode (ACM) controllers. Due to the bandwidth limitation, the VM control is not suitable for those converters with RHP zeros in their control transfer functions. The major benefits of ACM control are fast dynamic response and overload current protection. There are two types of ACM control schemes: namely analog and digital type. The analog controllers suffer from component ageing, temperature drifts, and they are also less accurate compared to the digital controllers. In spite of many drawbacks, the applications of analog controllers are limited to classical control theory for implementing simpler algorithms like

PI, PD, PID and compensation techniques. The digital controllers [21] can overcome all the above problems and provide stable performance for a wide range of line voltage and load variation. This paper addresses the design and implementation of QBC with digital ACM controller. The present SMPS design is focused on enhancing the switching frequency from several KHz to MHz. It offers several advantages such as high power packing density, low cost, good dynamic response, and prolonged lifetime due to the absence of electrolytic capacitors. However, the extreme high speed switching in power electronic converters results in excessive switch turn-on and turn-off losses, inductor core losses, and electromagnetic (EMI) noise issues.The conduction losses of inductor and capacitor will depend on the dc resistance (DCR) and the equivalent series resistance (ESR). The on-state drop of a power diode causes more conduction losses [26] and will affect the efficiency of the converter. Hence, the power diodes are replaced by schottky diodes at the penalty of increased cost. In order to improve the efficiency of the converter, the SR is [19] adopted in which the low-end MOSFET is realized in place of a schottky diode or a power diode. The mathematical analysis of losses in passive components and MOSFETs is explained in the succeeding sections.

The organization of this paper, in Section 2 modeling of the QBC is given. Section 3 describes the design of power components, switching frequency selection and efficiency analysis. Section 4 gives the digital ACM controller design. In Section 5 the simulation results and performance characteristics are presented. Finally, Section 6 gives the conclusions.

2. The Quadratic Buck Converter (QBC)

2.1 Voltage conversion ratio of QBC

The schematic of QBC [22], [23] is shown in Figure 1. It has one single switch and two LC filters. The voltage conversion ratio of QBC operating in continuous conduction mode (CCM) is represented by the Eq. (1).

$$M(D) = \frac{V_O}{V_{in}} = D^2 \tag{1}$$

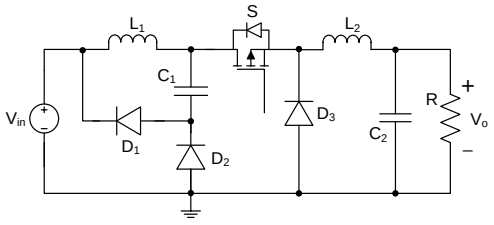

Fig. 1. Quadratic Buck Converter

To ensure CCM condition the values of L_1, C_1, L_2 and C_2 are selected as below.

$$\begin{aligned} L_1 &> \left(\frac{R(1-D)}{2D^2 f_{sw}}\right) \\ L_2 &> \left(\frac{R(1-D)}{2 f_{sw}}\right) \\ C_1 &> \left(\frac{D^2(1-D)}{2R f_{sw}}\right) \\ C_2 &> \left(\frac{(1-D)}{16 f_{sw}^2 L_2}\right) \end{aligned} \tag{2}$$

Where R is the load resistance, f_{sw} is the switching frequency, D is the nominal duty cycle of the converter, V_{in} & V_O are the input and output voltages of the QBC.

2.2 Basic operation

When the MOSFET switch 'S' is turned-on the diodes D_1 and D_3 are reverse biased, and also diode D_2 is forward biased. Then the source and capacitor C_1 pumps energy to the load through D_2 as shown in Figure 2.

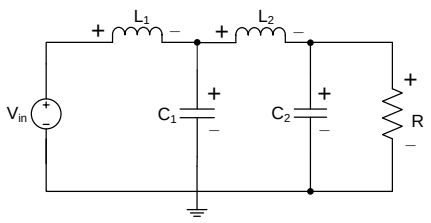

Fig. 2. QBC during turn-on

The equations governing the operation during turn-on are as follows:

$$L_1 \frac{dI_{L1}}{dt} = (V_{in} - V_{C1}) \tag{3}$$

$$C_1 \frac{dV_{C1}}{dt} = (I_{L1} - I_{L2}) \tag{4}$$

$$L_2 \frac{dI_{L2}}{dt} = (V_{C1} - V_{C2}) \tag{5}$$

$$C_2 \frac{dV_{C2}}{dt} = (I_{L2} - (V_{C2}/R)) \tag{6}$$

When the MOSFET 'S' is turned off, the diodes D_1 and D_3 are forward biased, and allows current through inductors L_1 and L_2. The diode D_2 remains reverse biased as shown in Figure 3.

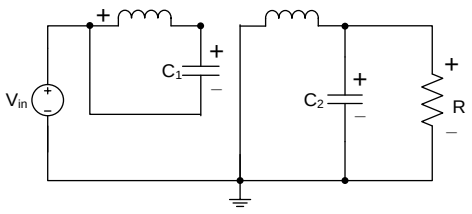

Fig. 3. QBC during turn-off

The equations governing the operation during turn-off are as follows:

$$L_1 \frac{dI_{L1}}{dt} = (-V_{C1}) \quad (7)$$

$$C_1 \frac{dV_{C1}}{dt} = (I_{L1}) \quad (8)$$

$$L_2 \frac{dI_{L2}}{dt} = (-V_{C2}) \quad (9)$$

$$C_2 \frac{dV_{C2}}{dt} = (I_{L2} - (V_{C2}/R)) \quad (10)$$

The I_{L1}, V_{C1}, I_{L2} and V_{C2} are the state variables considered for state space analysis, where I_{L1} & I_{L2} represents the currents through inductors L_1 & L_2 respectively, V_{C1} & V_{C2} represents the voltages across capacitors C_1 & C_2 respectively.

2.3 State-space modeling of QBC

Both the equilibrium model and the small-signal ac model [24], [25] are obtained by substituting the input quantity, state variables and state matrices in non-linear averaged equations given by Eq. (11).

$$k\frac{d\langle x\rangle_{Tsw}}{dt} = (D * A_1 + D' * A_2)\langle x\rangle_{Tsw} + (D * B_1 + D' * B_2)\langle u\rangle_{Tsw}$$
$$\langle y\rangle_{Tsw} = (D * C_1 + D' * C_2)\langle x\rangle_{Tsw} \quad (11)$$

The averaged matrices A, B, C & D are formed as:

$$A = A_1 D + A_2 D'$$
$$B = B_1 D + B_2 D'$$
$$C = C_1 D + C_2 D' \quad (12)$$

The equilibrium model is obtained by linearising about the steady state operating point and is represented as below.

$$0 = AX + BU$$
$$Y = CX \quad (13)$$

The following equations are obtained after linearising about the steady state operating point.

$$V_{C2} = D^2 V_{in}$$
$$V_{C1} = D V_{in}$$
$$I_{L1} = D I_{L2} \quad (14)$$
$$I_{L2} = D^2 (V_{in}/R)$$
$$I_{in} = D I_{L1}$$

The small-signal relationships between state variables can be derived by applying small-signal perturbations to the nominal input voltage V_{in} and to the nominal duty ratio D, these perturbations will result in variations in the state variables and the output voltage.

The linearised small-signal state equations are given by Eq. (15).

$$\hat{x} = (A_1 D + A_2 D')\hat{x} + (B_1 D + B_2 D')\hat{u} + \{(A_1 - A_2)X + (B_1 - B_2)U\}\hat{d}$$
$$\hat{y} = (C_1 D + C_2 D')\hat{x} + \{(C_1 - C_2)X\}\hat{d} \quad (15)$$

A linear model can be obtained by assuming the perturbations are sufficiently small such that the nonlinear terms are neglected and is given by Eq. (16).

$$\begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{D}{L_2} & -\frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1} & \frac{D}{L_1} \\ \frac{V_{C1}}{L_2} & 0 \\ -\frac{I_{L2}}{C_1} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{v}_{in} \end{bmatrix} \quad (16)$$

If the variations in input voltage V_{in} are negligible, they can be omitted in Eq. (16) by deleting the second column of matrix B. The negative aspect of linear time-invariant model [25] is that it not suitable for predicting sub harmonic oscillations due to ripple instabilities.

The transfer function of the control - to - input inductor current is given by Eq. (17).

$$\frac{\hat{i}_{L_1}(s)}{\hat{d}(s)} = \frac{V_{in}}{L_1} * \frac{a_1 s^3 + b_1 s^2 + c_1 s + d_1}{s^4 + a_2 s^3 + b_2 s^2 + c_2 s + d_2}$$
$$a_1 = (1),\ b_1 = (1/RC_2) \quad (17)$$
$$c_1 = (1/L_2C_2 + (2D^2/L_2C_1) + (D^2/R^2C_1C_2))$$
$$d_1 = (D^2/R^2C_1C_2)$$

The transfer function of the control - to - output voltage is given by Eq. (18).

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{DV_{in}}{L_2C_2}\left(\frac{s^2 - s(D^2/RC_1) + (2/L_1C_1)}{s^4 + a_2 s^3 + b_2 s^2 + c_2 s + d_2}\right)$$
$$a_2 = (1/RC_2),\ b_2 = (1/L_2C_2 + 1/C_1(1/L_1 + D/L_2)) \quad (18)$$
$$c_2 = 1/RC_1C_2[1/L_2 + D^2/L_2],\ d_2 = (1/L_1L_2C_1C_2)$$

The complex RHP zeros of Eq. (18) are given by:

$S = (\sigma \pm jw)$.

Where:

$$\sigma = \left(\frac{D^2}{2RC_1}\right) \qquad (19)$$

$$W = \sqrt{\frac{2}{L_1C_1} - \sigma^2}$$

From Eq. (19) it is evident that the undamped natural frequency of these zeros is independent of load and depends only on the parameters of the first stage of the converter. This transfer function has a non-minimum phase behavior and will affect the transient performance of the converter.

2.4 Power stage components design

The components L_1 and C_1 are designed using the Eqs. (20) & (22).

$$L_1C_1 < (2.222 * e - 011) \qquad (20)$$

$$L_1 = \left(\frac{D(1-D)V_{in}}{\Delta I_{L1} f_{sw}}\right) \qquad (21)$$

$$C_1 = \left(\frac{I_{L1}(1-D)}{\Delta V_{C1} f_{sw}}\right) \qquad (22)$$

The components L_2 and C_2 are designed using the Eqs. (23)-(25).

$$L_2 = \left(\frac{V_{in}D^2(1-D)}{\Delta I_{L2} f_{sw}}\right) \qquad (23)$$

$$C_2 = \left(\frac{V_{in}D^2(1-D)}{8\Delta V_{C2} f_{sw}^2 L_2}\right) \qquad (24)$$

$$\Delta V_0 = \Delta I_{L2}(ESR + DT_{Sw}/C_2) \qquad (25)$$

Figure 4 shows the I_{L1}, V_{c1}, I_{L2}, and V_{c2} waveforms and ensures CCM operation of the QBC.

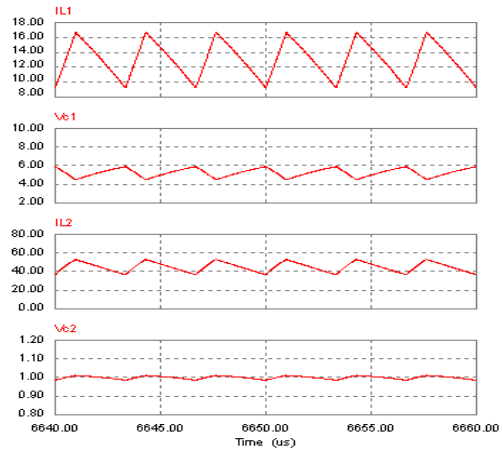

Fig. 4. Steady state waveforms of currents and voltages of inductors and capacitors

3. Switching Frequency effects & efficiency analysis of quadratic buck converter

Increase of switching frequency, gives the two fold benefit of improving not only the dynamic performance but also results in saving of space on the mother board. But the bottleneck is efficiency degradation [26], [27] of the QBC. It is seen that, for equal peak-to-peak ripple current, the inductor value is inversely proportional to converter switching frequency. This leads to low I^2R loss for the same core area since the number of turns gets reduced. However, the core loss in magnetic components will increase at higher switching frequencies. Hence, the advanced magnetic integration techniques are essential to minimize core losses. Also, for equal output ripple voltage, the capacitor value varies as the inverse of the switching frequency. But the detrimental effect is capacitor's ESR increases with a decrease in the capacitor value. Moreover, power electronic processors emit spurious electrical signals (EMI noise) causing self performance degradation in addition to interference with nearby electrical/electronic equipments. Besides, at very high switching frequencies (MHz), it is difficult to produce lower CPU core voltage of around 1V. Another major concern is the heat dissipation due to the number of constant energy switching events per time and necessitates a large heat sink. In order to enhance the lifetime of the battery the converter switching frequency should not exceed beyond 400 KHz. The industry usually targets efficiencies in the range of 80-85%.There should be a trade-off between efficiency and transient response.

3.1 Efficiency analysis of QBC

The conduction and switching losses are the dominant losses in a dc-dc converter. To minimise conduction losses, the DCR of the inductor and the ESR of the capacitor should be as low as possible. The SR is adopted to improve the efficiency of the converter. This is very specific for low output voltage and high current CPU voltage regulator module (VRM) applications [19]. There should be a trade-off between on-state resistance and gate charge of both upper and lower power MOSFETs.

3.1.1 Passive components and conduction losses

The inductor losses will depend on DCR of the winding and also on hysteresis phenomenon in the core magnetic material. A coil wire having a larger diameter can be used to reduce the conduction losses. In order to minimize core losses the converter should be operated at lower switching frequencies. But this necessitates a physically larger inductor at increased cost. However, this improves the efficiency of the converter.

The conduction loss of the capacitor will depend on the ESR.

The conduction loss of input side inductor L_1 can be computed as below:

$$P_{L_1} = (I^2_{L_1 rms} R_{L_1}) \quad (26)$$

Where:

$$I_{L_1 rms} = D I_O * \sqrt{1 + \frac{(\frac{\Delta I_{L1}}{D I_O})^2}{12}}$$

The conduction loss of inductor L_2 can be calculated as below:

$$P_{L_2} = (I^2_{L_2 rms} R_{L_2}) \quad (27)$$

Where:

$$I_{L_2 rms} = I_O * \sqrt{1 + \frac{(\frac{\Delta I_{L2}}{I_O})^2}{12}}$$

The conduction loss of input side capacitor C_1 can be computed as below:

$$P_{C_1} = (I^2_{C_1 rms} R_{C_1}) \quad (28)$$

Where:

$$I_{C_1 rms} = \sqrt{I^2_{2rms} + I^2_{3rms}}$$
$$I_{2rms} = \sqrt{D} * (I_{L_2 rms} - I_{L_1 rms})$$
$$I_{3rms} = \sqrt{(1 - D)} * (I_{L_1 rms})$$

The conduction loss [26] of output capacitor C_2 can be calculated as below:

$$P_{C_2} = \frac{R_{C_2} \Delta I^2_{L_2}}{12} \quad (29)$$

Where I_O is the load current, R_{L1} & R_{L2} are the DC resistances of L_1, & L_2, R_{C1} & R_{C2} are the ESR values of C_1 & C_2, ΔI_{L2} is the ripple in L_2, and I_{C1rms}, I_{C2rms}, I_{L1rms} and I_{L2rms} are the rms currents of capacitors and inductors respectively.

3.1.2 Diode conduction loss

The conduction loss in a power diode is largely affected by its forward voltage drop. The power diodes should be replaced by schottky diodes of very low on-state drop (~ 0.3V) and less reverse recovery time. But the overall cost of the converter increases.

The conduction loss [26] of schottky diode D_1 can be calculated as below:

$$P_{D_1} = (V_{F_1} I_{D_1 avg}) + (I^2_{D_1 rms} R_{D_1})$$
$$I_{D_1 avg} = D(1 - D) I_O \quad (30)$$
$$I_{D_1 rms} = D\sqrt{(1 - D)} I_O$$

The conduction loss of schottky diode D_2 can be computed as below:

$$P_{D_2} = (V_{F_2} I_{D_2 avg}) + (I^2_{D_2 rms} R_{D_2})$$
$$I_{D_2 avg} = D(1 - D) I_O \quad (31)$$
$$I_{D_2 rms} = (\sqrt{D})(1 - D)(I_O)$$

The conduction loss of schottky diode D_3 can be calculated as below:

$$P_{D_3} = (V_{F_3} I_{D_3 avg}) + (I^2_{D_3 rms} R_{D_3})$$
$$I_{D_3 avg} = D I_O \quad (32)$$
$$I_{D_3 rms} = (\sqrt{(1 - D)})(I_O)$$

Where I_{D1avg}, I_{D2avg} and I_{D3avg} are the average schottky diode currents, V_{F1}, V_{F2} and V_{F3} are the forward voltage drops of schottky diodes, and I_{D1rms}, I_{D2rms} and I_{D3rms} are the rms currents of schottky diodes respectively.

3.1.3 Upper power MOSFET loss analysis

The MOSFET conduction loss is proportional to the on-state resistance R_{on} and switching loss will depend on gate charge. For low voltage and high current applications [19], the Upper power MOSFET gate charge should be small and on-state resistance can be slightly higher. The conduction loss of upper power MOSFET can be computed as below:

$$P_{ConductionLoss,U-MOSFET} = I^2_{rms1} * R_{on1}$$
$$I_{rms1} = (\sqrt{D}) I_O \quad (33)$$

The switching loss [27] of upper power MOSFET can be calculated as below:

$$P_{SW,U-MOSFET} = \frac{V_{sw1} I_{pk1}}{2} f_{sw} (t_{s(L-H)} + t_{s(H-L)}) = \frac{V_{sw1} I_{pk1}}{2} f_{sw} (\frac{Q_{G1(sw)}}{I_{Driver(L-H)}} + \frac{Q_{G1(sw)}}{I_{Driver(H-L)}}) \quad (34)$$

$$I_{Driver(L-H)} = \frac{V_{DD} - V_{Qgd}}{R_{Driver(Pull-up)} + R_{Gate}}$$

$$I_{Driver(H-L)} = \frac{V_{Qgd}}{R_{Driver(Pull-down)} + R_{Gate}}$$

The gate power loss can be computed as below:

$$P_{Gate,U-MOSFET} = (Q_{Gsw1} V_{DD} f_{sw}) \quad (35)$$

The driver power loss can be computed as below:

$$P_{DriverLoss} = P_{Driver(L-H)} + P_{Driver(H-L)} = \left(\frac{R_{Driver(Pull-down)} P_{Gate}}{2(R_{Driver} + R_{Gate} + R_{Damping})} + \frac{R_{Driver(Pull-up)} P_{Gate}}{2(R_{Driver} + R_{Gate} + R_{Damping})}\right) \quad (36)$$

The output capacitor loss can be calculated as below:

$$P_{Coss} = \frac{V_{sw1}^2 C_{oss} f_{sw}}{2} \quad (37)$$

Where V_{sw} is peak switch voltage, I_{pk} is the peak switch current, R_{on} is the on-state resistance of MOSFET, R_G & R_D are the gate and driver resistances, C_{oss} is the MOSFET output capacitor and Q_G is the gate charge.

3.1.4 Lower power MOSFET loss analysis

The switching loss [27] of lower power MOSFET can be computed as below:

$$P_{SW,L-MOSFET} = (t_{2R} + t_{2F}) * V_{fd2} + \frac{(t_{3R} + t_{3F}) * (V_{fd2} * I_O * 1.1 * R_{ds2})}{2} * I_O * f_{sw}$$

$$K_{2R} = \left(\ln\left(\frac{V_{Driver}}{V_{Driver} - V_{p12}}\right) - \ln\left(\frac{V_{Driver}}{V_{Driver} - V_{th2}}\right)\right)$$

$$K_{3R} = \left(\ln\left(\frac{V_{Driver}}{V_{Driver} - (0.9 * V_{Driver})}\right) - \ln\left(\frac{V_{Driver}}{V_{Driver} - V_{th2}}\right)\right)$$

$$K_{2F} = \ln\left(\frac{V_{p12}}{V_{th2}}\right)$$

$$K_{3F} = \ln\left(\frac{0.9 * V_{Driver}}{V_{p12}}\right)$$

$$t_{2R} = K_{2R} * (R_{dr} + R_{gate}) * C_{iss}$$

$$t_{3R} = K_{3R} * (R_{dr} + R_{gate}) * C_{iss}$$

$$t_{2F} = K_{2F} * (R_{dr} + R_{gate}) * C_{iss}$$

$$t_{3F} = K_{3F} * (R_{dr} + R_{gate}) * C_{iss} \quad (38)$$

The switching loss of lower power MOSFET is neglected during turn-on and turn-off transitions because of the conduction of inherent body diode or an externally connected schottky diode.

The conduction loss of lower power MOSFET can be calculated as below:

$$P_{ConductionLoss,L-MOSFET} = I_{rms2}^2 * R_{on2}$$
$$I_{rms2} = (\sqrt{1-D}) I_O \quad (39)$$

The gate power losses can be computed as below:

$$P_{Gate,L-MOSFET} = (V_{DD} Q_{Gsw2} f_{sw}) \quad (40)$$

The reverse recovery loss can be calculated as below:

$$P_{rr} = (V_{sw1} Q_{rr2} f_{sw}) \quad (41)$$

The dead time is the time interval during which both the upper and lower MOSFETs are turned off, the lower MOSFETs body diode or an externally connected schottky diode will conduct. The power loss during dead time can be computed as below:

$$P_D = V_{fd2} I_0 f_{sw} (t_{Dead(R)} + t_{Dead(F)})$$
$$t_{Dead(R)} = t_{Delay(R)}$$
$$t_{Dead(F)} = (t_{Delay(F)} + t_{th}) \quad (42)$$
$$t_{th} = \frac{Q_G}{2 I_{LDRV}}$$
$$I_{LDRV} = \frac{V_{Driver} - \frac{V_{th}}{2}}{R_{Gate} + R_{Driver}}$$

The total losses of QBC can be calculated without and with SR as given below:

$$P_{withoutSR} = (P_{L_1} + P_{L_2} + P_{C_1} + P_{C_2} + P_{D_1} + P_{D_2} + P_{D_3} + P_{U-MOSFET}) \quad (43)$$

$$P_{WithSR} = (P_{L_1} + P_{L_2} + P_{C_1} + P_{C_2} + P_{D_1} + P_{D_2} + P_{U-MOSFET} + P_{L-MOSFET}) \quad (44)$$

The efficiency of QBC is computed as below.

$$\eta = \left(\frac{P_{out}}{P_{in}} * 100\right)$$

4. Digital average current-mode (ACM) controller

This paper presents the simulation of QBC with digital ACM [28-31] controller using PSIM software. Figure 5 shows the simulation diagram of QBC implemented with digital ACM controller.

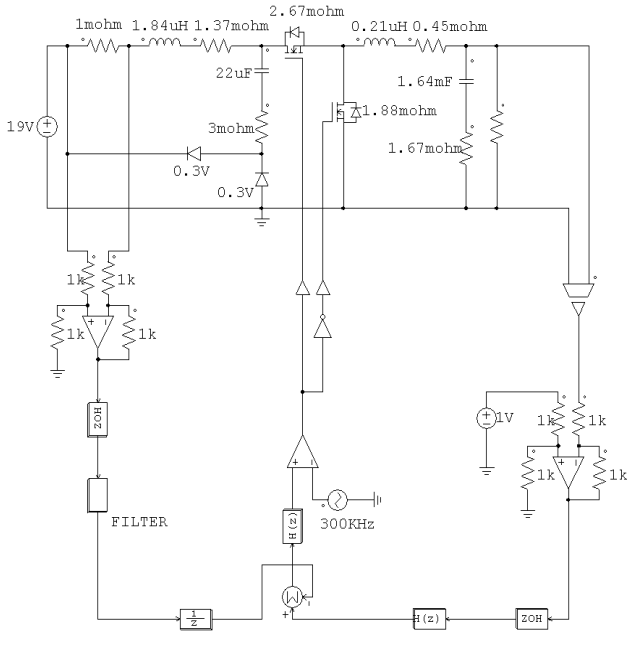

Fig. 5. QBC with Digital ACM controller

The transfer function of the current loop compensator, voltage loop compensator and the low pass filter in Z-domain are given by Eqs. (45)-(47).

$$C_1(Z) = (3.78 * (e + 010)) * \left(\frac{Z+1}{Z-1}\right) \quad (45)$$

$$C_2(Z) = \frac{(2Z^2 - 0.00045Z - 1.8)}{(Z^2 - 1)} \quad (46)$$

$$F(z) = \frac{Z+1}{(3Z-1)} \quad (47)$$

Initially, the controllers in both the inner current loop and the outer voltage loop are designed in the analog domain and then transformed into the Z-domain using Tustin's approximation. The coefficients of the digital controllers are finely tuned to get the desired steady state as well as transient performances.

5. Simulation results

The specifications of the QBC are shown in Table 1.

Table 1: Specifications of Quadratic Buck Converter

Quadratic Buck Converter	
Parameter	Nominal value
Input voltage	19 V
Inductor (L_1)	1.84µH
Inductor (L_2)	0.21 µH
DCR (L_1)	1.37mΩ
DCR (L_2)	0.45mΩ
Capacitor (C_1)	22µF
Capacitor (C_2)	1.64mF
ESR (C_1)	3.0mΩ
ESR (C_2)	1.67mΩ
Schottky diode FV drop	0.30V
Switching frequency	300kHz
Load resistance (min)	0.0333Ω
Output voltage	1V
Output power	30W

The following components are selected from on-line vendors of Mouser electronics, Digi-key and Coil-craft for QBC simulation. Upper-MOSFETs R_{on}=2.67mΩ (CSD17306QSA), Lower-MOSFETs R_{on}=1.88mΩ (CSD16414Q5), MOSFET driver (MCP14628 or FAN6520A), Schottky diode (MBRB2515L) forward voltage drop =0.3V, ΔI_{L1}=90%, ΔI_{L2}=40%, L_1 & L_2 (XAL1010) and C_1 (GRM31CR61E226KE15L or 19L), C_2 (EEF-SE0D561R).

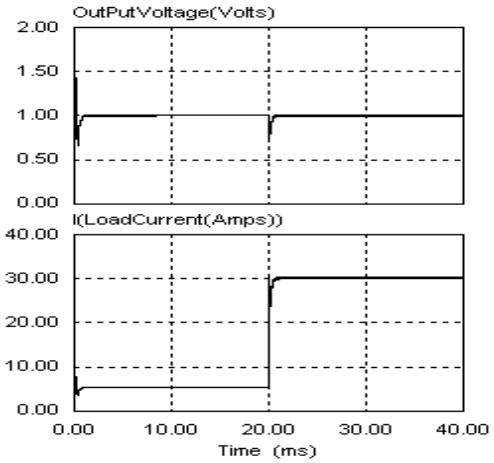

Fig. 6. Output voltage (1V) and load current (30A) waveforms of QBC with Digital ACM controller

Figure 6 shows the output voltage and load current waveforms for a step change in load (5A - 30A) at t = 20msec. The transient voltage deviation (TVD) is around 23% of rated output voltage (1V) and transient settling time (TST) is 0.75msec.The steady state voltage ripple (SSVR) is 1.0% of the rated output voltage (1V).

Figure 7 shows the output voltage and load current waveforms for a step change in input voltage from 19V-9V at t = 20msec, the TVD and TST are 26% and 2.5msec. Figure 8 shows the waveforms for a periodic change in load from 5A-30A and vice-versa. The TVD and TST are 20% (rise) & 0.75msec during a step decrease in load, also during step increase in load the TVD and TST are 17.5% (fall) and 2.5msec.

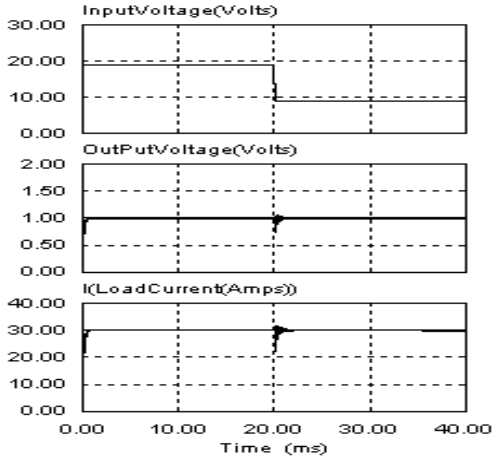

Fig. 7. Input voltage, output voltage (1V) and load current waveforms (30A) of QBC with Digital ACM controller

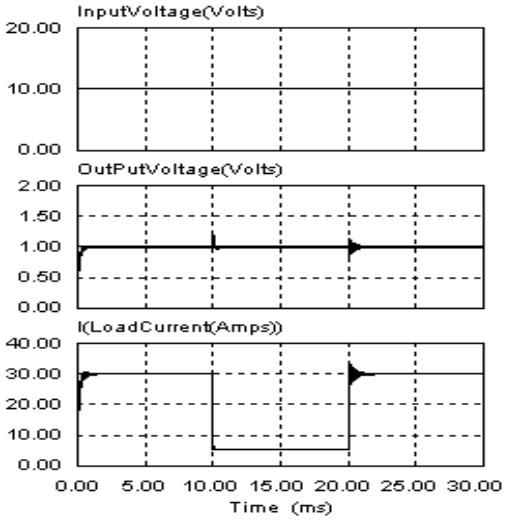

Fig. 8. Output voltage (1V) and load current (30A) waveforms of QBC with Digital ACM controller

Figure 9 shows the efficiency Vs load current without SR. The efficiency is calculated at different input voltages of 19V, 17V, 15V, 12V and 9V, the load current is varied in steps of 10A, 15A, 20A, 25A & 30A at f_{sw}= 300 kHz using MATLAB software. The maximum converter efficiency of 72.4075% is observed at V_{in}=9V & I_O=10A.The low converter efficiency of 70.3324% is observed at V_{in}=19V & I_O=30A. The change in efficiency is less at V_{in}=19V and comparatively more at 9V. It is evident that for a given input voltage the efficiency of the converter decreases as the load current increases.

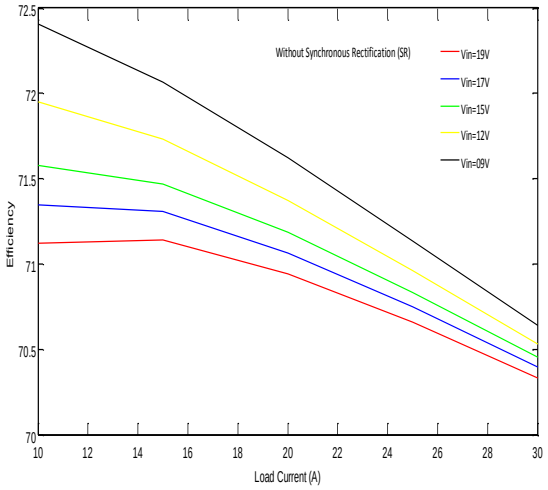

Fig. 9. Efficiency Vs load current without Synchronous Rectification (SR)

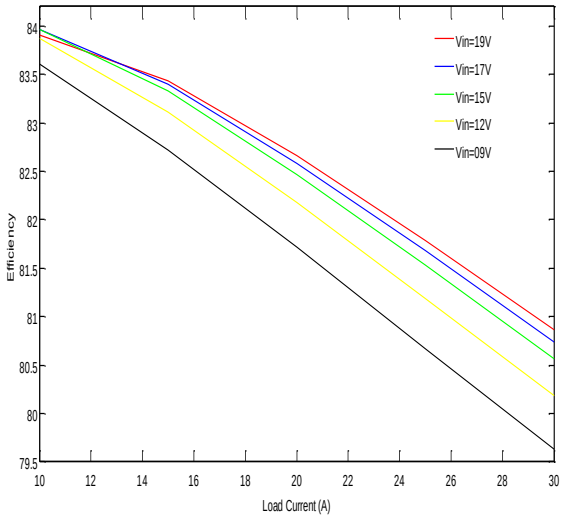

Fig. 10. Efficiency Vs load current with Synchronous Rectification (SR)

Figure 10 shows the efficiency Vs load current with SR. The efficiency is calculated at different input voltages of 19V, 17V, 15V, 12V and 9V, the load current is varied in steps of 10A, 15A, 20A, 25A & 30A at f_{sw}= 300 kHz. The maximum converter efficiency of 83.9684% is observed at V_{in}=15V & I_O=10A. The low converter efficiency of 79.6321% is observed at 9V & 30A. The change in efficiency is less at V_{in}=19V and comparatively more at 9V. It is evident that for a given input voltage the efficiency of the converter decreases as the load current increases.

Figure 11 shows the efficiency Vs duty cycle at different load currents of 10A, 20A, 30A & 40A, the output voltage is maintained constant at 1V. The minimum and maximum duty cycles are 0.18 and 0.33. The maximum efficiency of 83.9684% is observed at D=0.25 & I_O=10A. The low efficiency of 77.588% is observed at D=0.33 & I_O=40A. It is evident that for a given load current the efficiency decreases as the duty ratio varies. However, this change in efficiency with respect to duty cycle is less.

Figure 12 shows the efficiency Vs switching frequency at different load currents of 10A, 15A, 20A, 25A & 30A. The switching frequency of the QBC is varied from 100 KHz to 900 KHz at V_{in}=19V. The maximum converter efficiency of 86.5865% is observed at 100 KHz & 10A. The low converter efficiency of 75.0630% is observed at 900 KHz & 30A. It is observed that for a given load current the efficiency of the converter decreases with an increase in the switching frequency of the converter.

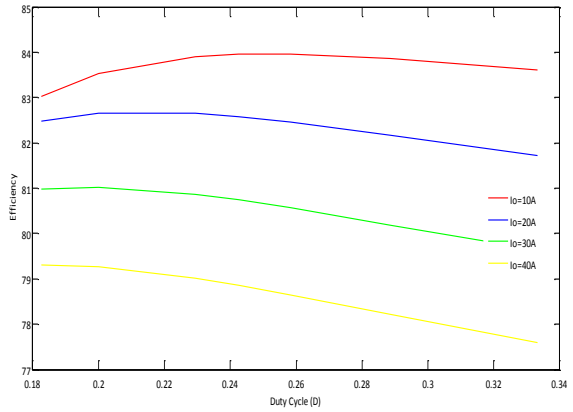

Fig. 11. Efficiency Vs Duty cycle at different load currents & V_{in}=19V

At rated load current of 30A, for the variation of switching frequency from 100 KHz to 900 KHz the efficiency changes by 7.5605%. For the switching frequency variation from 100 KHz to 300 KHz & 300 KHz to 500 KHz the efficiency changes by 1.757% and 2.0215% respectively. The maximum efficiency change of 10.139% is observed at 10A. As the industry usually targets efficiencies in the range of 80-85%, the efficiency degradation of 0.5-1.0% are accountable as it is difficult to achieve converter efficiencies beyond 80% at load currents exceeding 30A. So, 300 KHz is the preferable switching frequency for low voltage and high current applications.

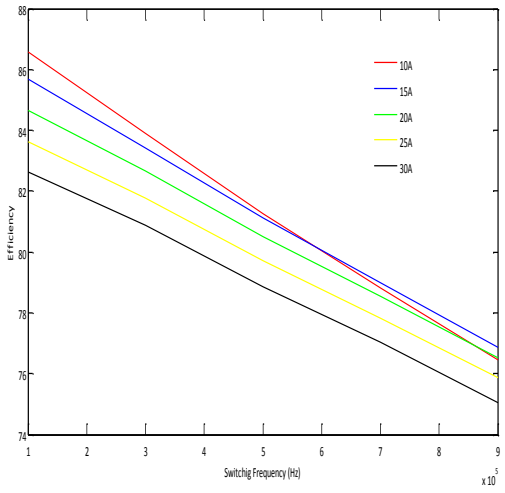

Fig. 12. Efficiency Vs Switching frequency at different load currents & V_{in}=19V

Figure 13 shows the bar diagram representing the variation of conduction loss, switching loss, reverse recovery loss, output capacitor loss and gate loss of QBC at different switching frequencies.

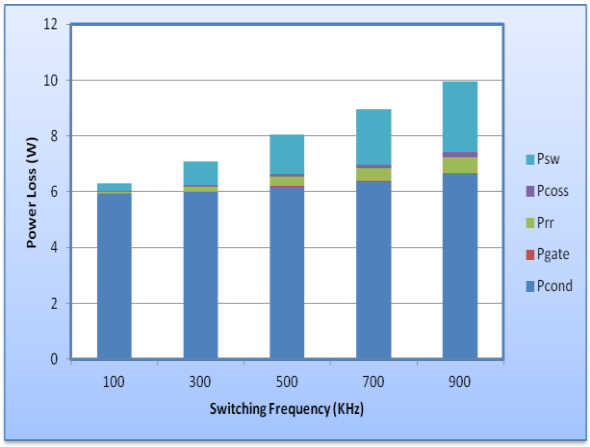

Fig. 13. Bar diagram representing various losses of QBC

6. Conclusions

In this paper the low frequency model of the QBC is presented using state-space averaging technique. The QBC is implemented with digital ACM control strategy and the simulated waveforms of load voltage (1V) and load current (30A) are shown. The TVD is around 23% of rated output voltage (1V) and TST is 0.75msec, with a SSVR of 1.0% of the rated output voltage (1V). The efficiency Vs load current characteristics of QBC are presented for different input voltages with and without SR. At rated load current of 30A, the SR improves the efficiency of the converter by 10.5341%. Also, the performance characteristics of the QBC such as efficiency Vs switching frequency and efficiency Vs duty cycle are represented. For switching frequency variation from 100 KHz to 300 KHz & 300 KHz to 500 KHz the efficiency of QBC changes by 1.757% and 2.0215% respectively. Thus, the preferable switching frequency is 300 KHz, a compromise worked out between converter efficiency and transient response.

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