# COMPARATIVE STUDY OF SWITCHED-MODE POWER SUPPLIES FOR LOW VOLTAGE AND HIGH CURRENT APPLICATIONS

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***Abstract:*** *Future generation microprocessor poses many challenges to its dedicated power supplies for delivering high quality power, the voltage regulators (VRs), such as very low voltage, high currents, faster load transitions and tight voltage regulation. Also the power management issues in computing systems are becoming complex and fixing remarkable targets for the design engineers. This paper presents broad review on different dc-dc converter topologies like multi-phase synchronous buck, multiphase non - coupled and coupled-inductor buck, asymmetrical half-bridge converter with current doubler and the duty cycle extended quadratic buck converter (QBC). The design, control and simulation of each converter are presented for 1V/30A at a switching frequency of 300 kHz. The simulation of each converter is performed in closed-loop mode using PSIM software and the performance of different topologies is compared in terms of transient voltage deviation, transient settling time, steady state voltage ripple, estimated cost and efficiency.*

***Key words:*** *Quadratic buck converter (QBC), voltage-mode control, average current-mode controller (ACM), transient settling time (TST), transient voltage deviation (TVD), steady state voltage ripple (SSVR), synchronous rectification (SR), inherent body diode (IBD).*

## 1. Introduction

In day-to-day life the usage of mobile laptop computers is increasing and gaining most of the market share than the desktop computers. The laptop computer uses mobile microprocessor that operates at higher clock frequencies for faster computations and increases the power consumption [1]. In order to reduce the power consumption, the advanced microprocessors should operate at very low voltages (around 1V) with very tight voltage regulation [2]. However, works are focused on optimizing the voltage regulator to achieve adaptive voltage position (AVP) during the load transients. In this adjusting the bus voltage according to the load current, the system efficiency can be optimized for the whole load range. According to Intel's road map [3], over one billion transistors will be integrated in one processor; the processor's clock speed will approach from few MHz to GHz. The microprocessors will run at very low voltage (below 1V), will consume up to 100A of current, and will have dynamics of about 400A/µs. The multiphase interleaving synchronous buck [4]-[7] topology is widely used in today's laptop computer applications as a voltage regulator (VR). In general a battery, fuel cell or a PV-module can be used as power sources for laptop computer. Also as fuel cells are very sensitive to current ripples, for continuous and stable operation of ABFC or PEM fuel cell, the average input current of the dc-dc power converter should be controlled to obtain smoother dc. The output voltage of AC adapter is 19V dc obtained from single phase AC voltage of 230V in countries like India. So, the CPU voltage regulator (VR) needs to convert its 9~19 V input voltages to the output CPU core voltage of 1V. Thus the VR should be able to meet line voltage regulation as well as load current regulation. For low CPU core voltages the duty cycle of the buck converter becomes extremely small. The problems associated with narrow duty cycle are reduced switching frequency because of minimum turn-on time requirement of the switch and increased peak switch current that leads to more switching losses. A two-stage buck converter [8] uses two buck converters in cascade and operates at higher switching frequencies with wide load range over the entire input voltage range. It gives better efficiency than single stage and is suitable only for low level currents as efficiency degrades at higher load currents. The tapped-inductor buck converter [9] even though extends converter duty cycle, suffers from leakage inductance, voltage spikes across top switch, requirement of transformer-isolated or opto-isolated gate drive, and increased switching losses may destroy the top-switch. Other topologies were also suggested to reduce leakage-energy problem. In active-clamp circuit two extra coupled windings and in passive-clamped circuit a third winding is to be incorporated. In modified tapped inductor buck converter with a lossless clamp [10] circuit uses bootstrap gate driver, leakage energy is recovered,

simple structure, smaller in size and low cost. The active-clamp couple buck converter [11] gives larger duty ratio, recovery of leakage energy, clamped device voltage and input filter inductance is reduced. But the magnetic circuit design becomes complex. The non-isolated forward topology [12] extends duty cycle, reduced switching losses and conduction losses. But the drawbacks are increase in transformer size, first quadrant operation of B-H curve and also the voltage stress becomes double on the primary switch. The non isolated push-pull buck converter [13]-[15] extends duty cycle, improves both efficiency and transient performance, and for the same output power smaller core area is required compared to the forward topology. But the transformer design becomes complicated as it needs two windings on the primary, double the voltage stress and also transformer imbalance is the dominant issue. The non-isolated half-bridge [16]-[18] topology with current doubler extends duty cycle, smaller size transformer compared to forward topology, voltage stress same as input voltage and control technique is simple. Even though the non-isolated double-ended topologies use less transformer turns ratio compared to isolated topologies, they have more switching loss, conduction loss and also reverse recovery loss in synchronous switch, limits their usage for low current applications. Various methods [19]-[23] are suggested to improve performance of different topologies in terms of transient voltage deviation (TVD), transient settling time (TST), without compromising for efficiency. This paper presents broad review on different topologies like multi-phase synchronous buck, multiphase non-coupled and coupled-inductor buck converter, asymmetrical half-bride converter with current doubler and the quadratic buck converter (QBC). The dynamic as well as steady state performance of these topologies are compared. The power circuit architecture, design and their control are explained in section 2. Section 3 presents the simulation results and finally conclusions are stated in section 4.

## 2. Converter topologies

### 2.1 Multi-phase buck converter

The multi-phase buck converter is widely used in laptop Voltage Regulator Module (VRM) applications because of its low cost and simplicity. But this topology has the drawbacks of narrow duty cycles when it operates at higher switching frequencies, for extremely low CPU core voltages of around 1V. The multi-phase synchronous buck converter [5], [24] uses interleaved timing to multiply ripple frequency to reduce the input and output currents. The current ripple cancellation results in lower cost of output capacitors, fewer components and reduced power dissipation. The power consumption of a typical microprocessor is given as $P=CV^2f$. As power consumption is proportional to the switching frequency, the thermal and battery life constrain in the laptop limits the switching frequency of the power converter, the design engineers in industry usually targets for 85% efficiency for processor applications and the switching frequency cannot exceed 350 kHz. This limitation will affect the transient performance of the converter. However with the necessity of complex and fast computations, the switching frequency has to be raised to MHz. A compromise between efficiency and transient performance is necessary. It can be seen that there is a critical inductance $L_{cr}$, the largest inductance that yields the best transient response. The critical value of inductance for individual phase is given by Eq. (1).

$$L_C = \frac{V_o}{4.\Delta I_o.f_c}.\Delta D_{max} \quad (1)$$

Where $V_{in}$ is the input voltage, $\Delta I_o$ is the maximum current change, $f_C$ is the control bandwidth and $\Delta D_{max}$ is the maximum allowed duty cycle change. The synchronous rectification (SR) is used to improve the efficiency of the converter. Figure 1 shows the basic block diagram of N interleaved synchronous buck phases [24] with voltage-mode hysteretic control and simulation results for 4-phase are presented.

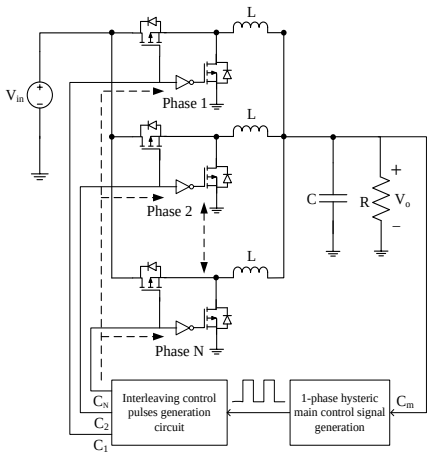


Fig. 1. Block diagram of N phase interleaved buck converter with voltage-mode hysteretic control

Where $C_m$ is the main control signal, $C_1$ & $C_2$ are the phase 1 and phase 2 control signal, in general $C_N$ is the phase N control signal. The VM hysteretic control is more versatile compared to other control techniques such as simplicity, no feedback loop compensation requirement, good dynamic performance and no limitation on the switch conduction time. On the other hand, the interleave technique has several benefits such as high frequency output voltage ripple with lower

switching frequency, ripple cancellation, higher current carrying capability, and also fast transient response which is limited by the feedback control loop. Combining the merits of these two control strategies provides good results.

### 2.2 Multiphase Coupled-inductor Buck Converter

The conflict between high efficiency and fast transient response in multiphase interleaving buck converter is overcome by multiphase coupled-inductor buck converter [25]. The coupled-inductor works as a nonlinear inductor due to the phase-shifted switching network. The coupled-inductor has different equivalent inductances during steady-state and transient conditions. In steady state the inductance is increased due to coupling and efficiency of multiphase coupled-inductor buck converter is increased. On the other hand, during step-up or step-down load transients the inductance is reduced, the transient performance of the converter is improved. However the multiphase coupled-inductor buck converter in reality is not symmetric. C. Sullivan analyzed the n-phase (n>2) symmetric coupled-inductor buck converter when the duty cycle D is less than 1/n. The performance of n-phase (n>2) symmetric coupled-inductor buck converter with D>1/n is still nebulous. For D<1/n the steady state and transient reactance's are given by Eqs. (2) & (3).

$$L_{SS} = \frac{(L-M)[L+(n-1)M]}{L+[(n-2)+(n-1)\frac{D}{D'}]M} \qquad (2)$$

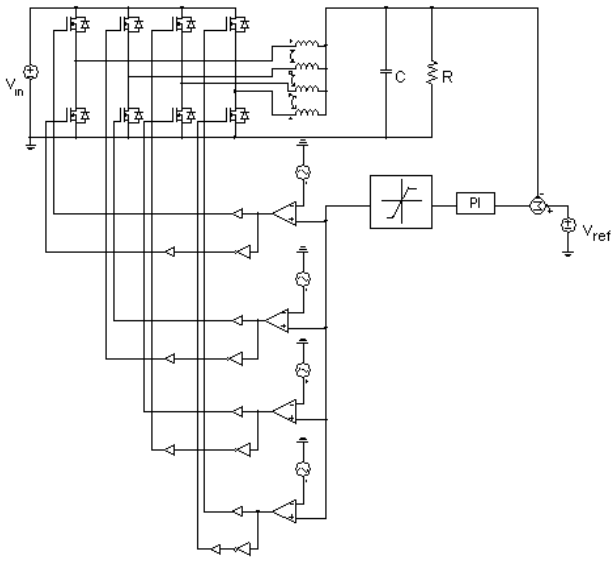


Fig. 2. Schematic of 4-phase coupled-inductor buck converter with voltage-mode (VM) controller

$$L_{tr} = L+(n-1)M \qquad (3)$$

Figure 2 shows the simulation circuit of 4-phase coupled-inductor buck converter with voltage-mode (VM) controller. However the exhaustive analysis of the converter, current sensing and light-load efficiency enhancement are the challenging issues for this topology. It can be seen that the multiphase coupled-inductor buck has a much lower efficiency at light load conditions than the multiphase non-coupled inductor buck converter.

### 2.3 DC-DC Isolated topologies

On the other side the different dc-dc isolated topologies [26] are two-switch forward converter, phase shift full-bridge converter and the half-bridge converter. In two-switch forward converter two primary switches are not connected in totem pole configuration, solve the shoot through problem. The major disadvantages of this topology are large filter inductor, low efficiency and hard switching, not suitable for high frequency operation. But in half-bridge and full-bridge converters, the primary switches are connected in totem pole structure. The phase shift full-bridge converter [26] is a soft switching converter that achieves Zero Voltage Switching (ZVS) with high frequency operation, and lower volt-sec on the output filter inductor. But the disadvantages are more complex driver circuit and large leakage inductance requirement for achieving ZVS. The large leakage inductance requirement may affect the dynamic performance of the whole converter. Finally it is not the preferable one for laptop VRMs requiring extremely small duty ratios, leads to more circulating current and higher conduction loss.

The symmetrical half-bridge [26], [18] is a hard switching topology and leakage inductance will denigrate the performance of converter. So the output power range is limited. The asymmetrical half-bridge (HB) is a soft switching converter and can achieve ZVS with the help of leakage inductance. There is no ringing problem caused by leakage inductance and no circulating current as seen in phase shift full-bridge converter. But the drawbacks are voltage stress on the secondary rectifier and output filter diodes, limits the choice of diodes. The current doubler is a topology for secondary rectifier and is widely used for low voltage and high current applications because of reduced transformer winding losses, higher efficiency and high power density with magnetic integration. Figure 3 shows the schematic of asymmetrical HB with current doubler.

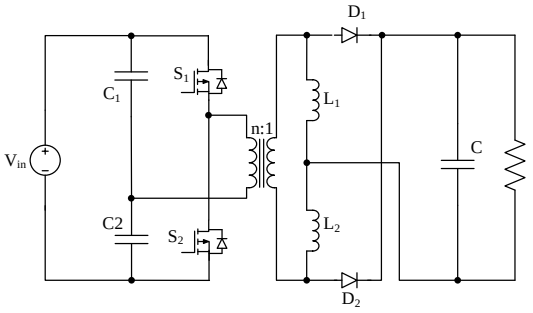


Fig. 3. Schematic of asymmetrical HB with current doubler

However higher efficiencies are not possible with this topology due to high conduction losses. Figure 4 shows its modified circuit with synchronous rectification (SR) which can improve the efficiency of the converter by reducing conduction losses due to diodes. In synchronous rectification the diodes are replaced by MOSFETs at increased cost. During dead time when the synchronous rectifier is turned off, there is a current flow through the IBD of MOSFET. Since the IBD of MOSFET is very slow, the reverse recovery current will be higher and causes voltage ringing on the synchronous rectifier. The quasi square wave (QSW) synchronous rectification [26] technique reduces conduction loss, can achieve zero voltage switching (ZVS) in primary switches at whole load range and prevents conduction of body diode of synchronous rectifier. When voltage stress is lower than 200V, synchronous rectifier is beneficial compared to diode rectifier, however this limitation can be overcome with advanced power MOSFET technology. The other drawback is high turn-off current in primary switches which increases the switching losses, not suitable for higher switching frequencies beyond 400 KHz.

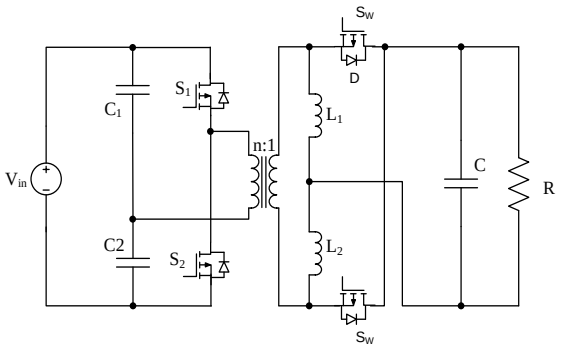


Fig. 4. Schematic of asymmetrical HB CD with SR

As the leakage inductance is detrimental to the performance of the HB converter, it can be improved by connecting buck converter across asymmetrical half-bridge (HB) converter with current doubler as shown in Figure 5. The buck converter engages only during transient periods, it supplies the fast rising or falling transient load currents at the converter output as shown in Figure 6.

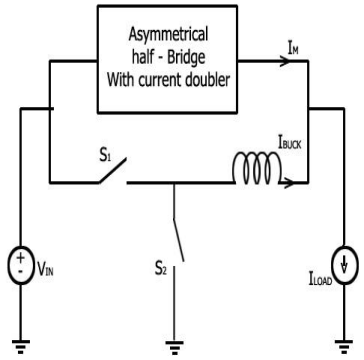


Fig. 5. Asymmetrical half-bridge converter with current doubler, buck converter in parallel

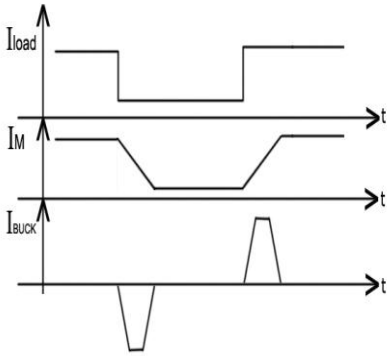


Fig. 6. Buck current during load current transitions

For asymmetrical half-bridge, the input and output voltage relationship in terms of turn's ratio is given by Eq. (4).

$$V_O = \frac{V_{in} D(1-D)}{n} \tag{4}$$

For a given input voltage $V_{in}$, output voltage $V_o$, turns ratio 'n' and switching frequency $f_{sw}$, the inductor value of the CDR is given by Eq. (5).

$$L_1 = L_2 = \frac{V_O (1-D)}{f_{sw} \Delta I_{L_1}} \tag{5}$$

Where D is the steady-state duty cycle calculated at the maximum input voltage (19 V) and $\Delta I_L$ is the peak-peak ripple current of the inductor (taken as only 10-20% of inductor current at full-load current).The proposed control scheme [27], [28] is shown in Figure 7 for asymmetrical HB with current doubler and buck converter in parallel.

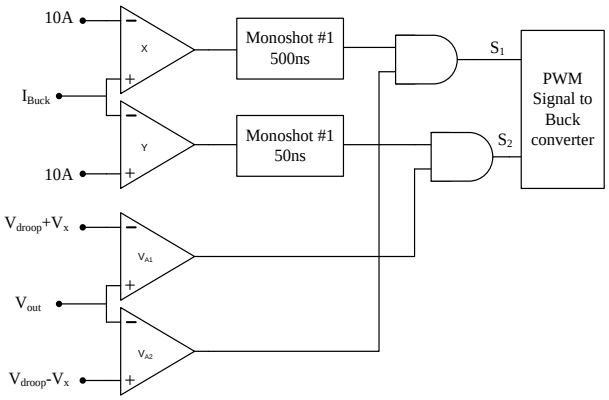


Fig. 7. Simplified diagram of the proposed control scheme (Hysteretic constant turn-off control)

The control scheme design is based on the boundaries of a threshold band ($2V_x$) on the actual voltage reference ($V_{droop}$). If the output voltage is within the allowable threshold band, only the asymmetrical HB with current doubler operates. If $V_o$ exceeds the threshold band, the buck converter will turn-on and supplies the transient currents, improves the dynamic performance.

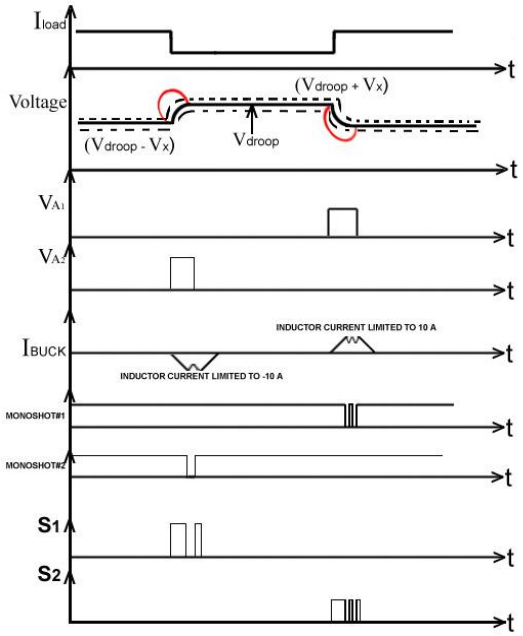


Fig. 8. Operating waveforms of hysteretic constant turn-off control

In Figure 8 '$V_{A1}$', '$V_{A2}$' and 'X', 'Y' are the voltage and current comparators respectively. When the output voltage deviates from '$V_{droop}$' by 20mV ($V_x$) i.e. for step-up load transient, the output of the comparator '$V_{A1}$' becomes high, switch '$S_1$' is turned ON and it gets turned OFF when the output voltage falls into the threshold band or when the inductor current of the buck converter reaches the current limit of 10A. A constant turn-off period of 500ns is maintained for the switch '$S_1$' by a monoshot circuit and for step-down load transient the switch '$S_2$' is controlled instead of switch '$S_1$'.

### 2.4 Quadratic buck converter

The quadratic buck converter [29] is suitable for very low voltage applications because of its voltage conversion ratio has a quadratic dependence on duty cycle. The schematic of QBC is shown in Figure 9.The conversion ratio of QBC is represented by the Eq. (6).

$$M(D) = \frac{V_O}{V_{in}} = D^2 \tag{6}$$

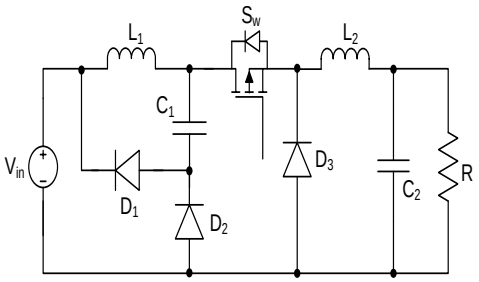


Fig. 9. Quadratic buck converter (QBC)

The resonant frequency of the complex zeros in the RH plane depends on $L_1$ and $C_1$ and given by

$$W_r = \sqrt{\frac{2}{L_1 C_1}}$$

As this frequency limits the control bandwidth, the parameters can be selected such that the resonant frequency of complex zeros should be higher than the control bandwidth. The designed values of $L_1$ and $C_1$ are obtained by using the following Eqs. (7) & (8).

$$L_1 = \left(\frac{V_{C1}(1-D)}{\Delta I_{L1} f_{sw}}\right) \tag{7}$$

$$C_1 = \left(\frac{I_o D(1-D)}{\Delta V_{C1} f_{sw}}\right) \tag{8}$$

The designed values of $L_2$ and $C_2$ are obtained by using the following Eqs. (9)-(10).

$$L_2 = \left(\frac{V_o(1-D)}{\Delta I_{L2} f_{sw}}\right) \quad (9)$$

$$C_2 = \left(\frac{V_o(1-D)}{8\Delta V_{C2} f_{sw}^{\ 2} L_2}\right) \quad (10)$$

The output capacitor ripple $\Delta V_{C2}$ and inductor current ripple $\Delta I_{L2}$ allowed are 2% and 30% respectively. Similarily $\Delta V_{C1}$ and $\Delta I_{L1}$ are 20% and 40%.

In literature there exists the following control strategies for switched-mode power supplies (SMPS): voltage-mode (VM) control, peak current-mode control, average current-mode (ACM) control and the sliding-mode (SM) control. In continuous conduction mode (CCM) operation of QBC, the control-to-output voltage transfer function with two RHP zeros will debilitate the control bandwidth and causes poor dynamic response. This problem is exaggravated particularly with VM controllers. This narrow gain bandwidth limitation of VM control can be rectified with ACM controller. Figure 10 shows the schematic of QBC with ACM controller.

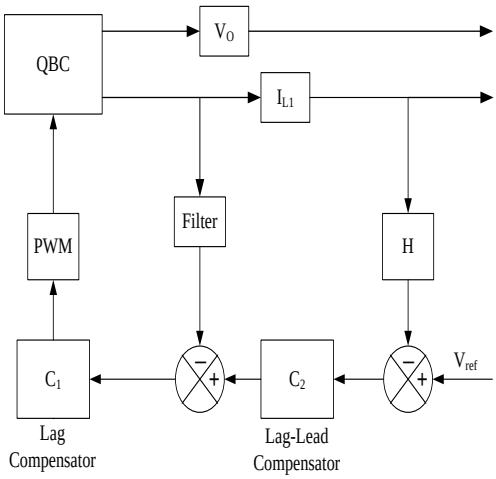


Fig. 10. Block diagram of average current-mode (ACM) controller

In this, an inner current loop is present in addition to the outer voltage loop. Due to bandwidth separation, the current loop has fast dynamics compared to the voltage loop (slow dynamics). The ACM control [30]-[32] has several features than peak current-mode control such as better accuracy, good noise immunity, no need for slope compensation and overload current protection. The power converters are highly non-linear and can be described as a time-variant system. The linear control strategies discussed above are not omnipotent to achieve robustness against system parameter variations. In such conditions the sliding-mode (SM) control is the better choice as its control-law does not depend on system dynamics, the control action depends on the parameters of the switching function only. The traditional SM controllers require variable switching frequencies which is unacceptable in many applications because of electromagnetic interference (EMI). The most preferable solution for this problem is to adapt a hysteresis loop in switching element to fix or further to control the switching frequency. The Hysteresis control is widely used for dc-dc converters, identical to ideal SM control with hysteresis loop width tending to zero.

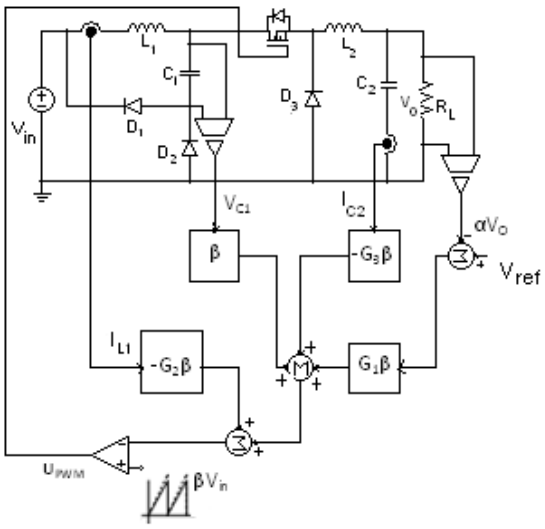


Fig. 11. Block diagram of sliding-mode (SM) current controller

The ideal robustness is possible only when the converter operates at infinite switching frequency. Although modern power semiconductor devices have the ability to operate at higher switching frequencies, this operation is not allowable due to high heat losses in power converters. In order to achieve robustness against line and load regulations, a fast response fixed frequency PWM based SM current controller [33], [34] is designed for QBC as shown in Figure 11. The salient features of SM current controller are good dynamic performance, inherent robustness and stable over a wide range of operating conditions compared to conventional current-mode controllers even if the converter is designed at nominal conditions. But the drawback is its perplex architecture and requirement of more number of current and voltage sensors compared to conventional control schemes. The SM controller implementation includes designing of a switching function and then selection of control law that

makes the switching function attractive to the state of the system. The instantaneous state variable's trajectory is given by Eq. (11).

$$s = k_1 x_1 + k_2 x_2 + k_3 x_3 \tag{11}$$

The state variables $x_1$, $x_2$ and $x_3$, are expressed as

$$\begin{aligned} x_1 &= (i_{ref} - i_{L_1}) \\ x_2 &= (V_{ref} - V_0) \\ x_3 &= \int (i_{ref} - i_{L_1})dt + \int (V_{ref} - V_0)dt \end{aligned} \tag{12}$$

The equivalent-control signal of the SM current controller for quadratic buck converter is obtained by solving $\dot{s} = 0$.

The equivalent-control signal [33], [34] is given as

$$u_{eq} = \frac{V_{C1}}{V_{in}} + G_1 \frac{(V_{ref} - \alpha V_0)}{V_{in}} - G_2 \frac{i_{L1}}{V_{in}} - G_3 \frac{i_{C2}}{V_{in}} \tag{13}$$

The simulation results for both ACM and SM current control strategies are presented in the succeeding sections.

## 3. Simulation results

The silicon schottky diodes are widely used for dc-dc converter applications because of their low forward voltage drop, fast reverse recovery and reduced conduction losses compared to ordinary silicon PN junction diodes or power diodes. This increases the efficiency of the converter but they are more expensive. The efficiency is further increased by replacing the schottky diode with a low side MOSFET performing synchronous rectification (SR). During dead time periods the inherent body diode (IBD) of MOSFET which has a very slow reverse recovery characteristic can affect the efficiency of the converter. So to overcome this problem an external schottky diode can be placed in parallel with the low-side FET to shunt the IBD. The simulation results of different converter topologies and their efficiency comparison are presented with silicon PN junction diodes or power diodes, schottky diodes and with synchronous rectification (SR).

The specifications of different topologies for same input and output conditions i.e $V_{in}$ =19V, $V_o$=1V, $I_o$= 30A and $f_{sw}$=300 kHz are given below, obtained from the data sheets of the respective manufacturers. For multi-phase (4-phase) buck converter the output capacitor $C_o$=1000µF (ESR=5.0mΩ), inductance per phase L=3µH ($R_{dc}$=4.47mΩ), MOSFETs $R_{on}$=2.3mΩ, SR MOSFETs $R_{on}$=2.3mΩ, forward voltage drop (FVD) of power diode and schottky diode are 1V & 0.35V. For multiphase non-coupled (4-phase) buck converter $C_o$=1000µF (ESR=5.0mΩ), inductance per phase L=0.402µH ($R_{dc}$=6.05mΩ), MOSFET $R_{on}$=2.3mΩ, forward voltage drop (FVD) of power diode and schottky diode are 1V & 0.35V. For multiphase coupled (4-phase) buck converter $C_o$=1000µF (ESR=5.0mΩ), self-inductance $L_s$=40nH ($R_{dc}$=1.55mΩ), MOSFETs $R_{on}$=2.3mΩ, mutual inductance $L_m$=620nH, forward voltage drop (FVD) of power diode and schottky diode are 1V & 0.35V. For asymmetrical HB with CD $C_o$=1000µF (ESR=5.0mΩ), $C_1$=$C_2$=90uF (ESR=3.0mΩ), $L_1$=$L_2$=650nH ($R_{dc}$=1.93mΩ), MOSFETs $R_{on}$=2.3mΩ, SR MOSFETs $R_{on}$=2.4mΩ, forward voltage drop (FVD) of power diode and schottky diode are 1V & 0.38V. Similarly for QBC $L_1$=1.84µH ($R_{dc}$=2.30mΩ), $L_2$=0.21µH ($R_{dc}$=0.65mΩ), $C_1$=22µF (ESR=3.0mΩ), $C_2$=1.67mF (ESR=1.67mΩ), MOSFETs $R_{on}$=2.3mΩ, SR MOSFETs $R_{on}$=2.4mΩ, power diode and schottky diode forward voltage drops are 1V, 0.35V & 0.38V.

Figure 12 shows the output voltage and load current of 4-phase synchronous buck converter, for a step-change in load from (5A-30A), the output voltage undergoes a TVD of 9% (fall) and TST of 1.3msec. As shown in Figure 13 for 4-phase non-coupled inductor buck converter and for the same load change the TVD and TST are 14% (fall) & 0.4msec, in case of 4-phase coupled inductor buck converter as shown in Figure 14 the TVD and TST are 18% (fall) & 0.05msec. Figure 15 shows the output voltage, buck current and load current of asymmetrical HB with current doubler, without and with buck converter in parallel. Figure 16 shows output voltage and load current of asymmetrical HB with current doubler, without buck and for step-down load transient i.e. from (30A-5A) the TVD and TST are 20% (rise) & 0.06msec, and with buck the TVD and TST are 10% (rise) & 0.025msec. Similarly as shown in Figure 17, without buck and for step-up load transient, the TVD and TST are 5% (fall) & 0.3msec, and with buck the TVD and TST are 5% (fall) & 0.02msec. Figure 18 shows the output voltage and load current of QBC with ACM controller, for a step-change in load from (5A-30A), the TVD and TST are 20% (fall) & 0.6msec. Figure 19 shows the simulation results of QBC with SM current controller, the TVD and TST are 6% (fall) and 5.0µsec.

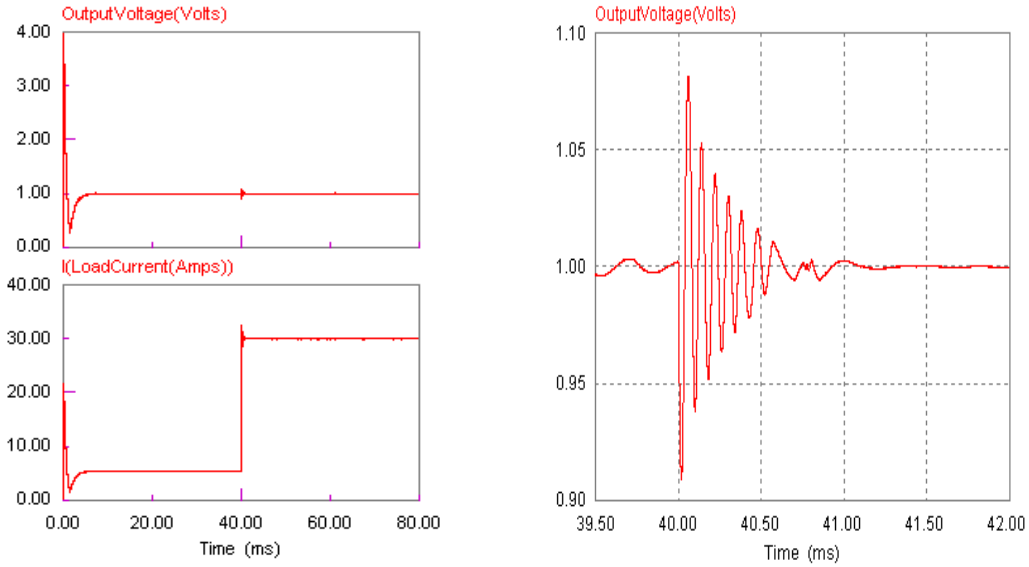


Fig. 12. Output voltage and load current of 4-phase synchronous buck converter

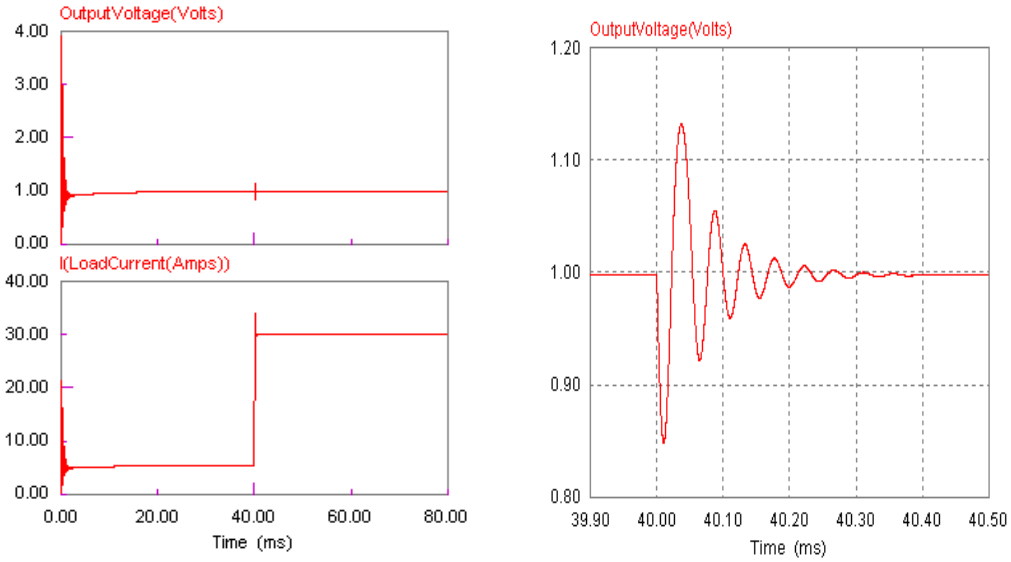


Fig. 13. Output voltage and load current of 4-phase non-coupled inductor buck converter

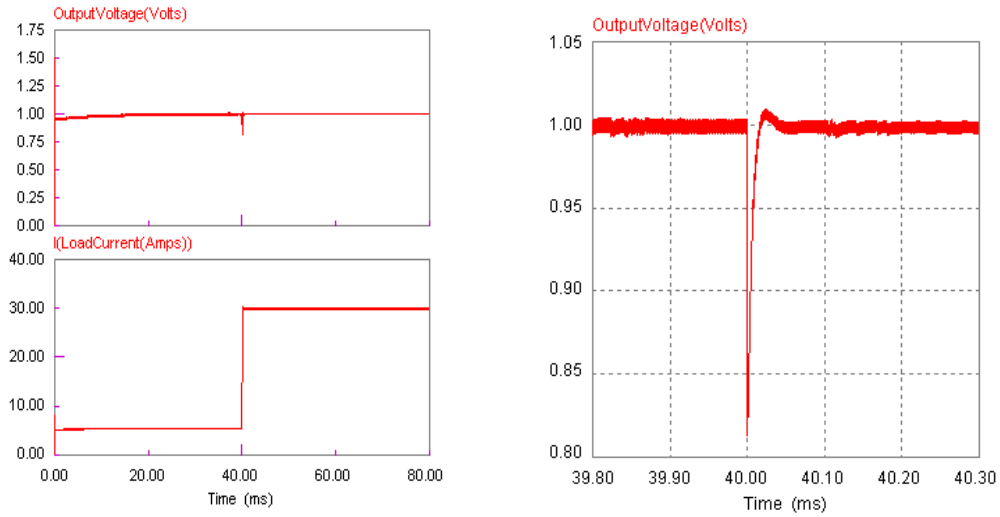


Fig. 14. Output voltage and load current of 4-phase coupled-inductor buck converter

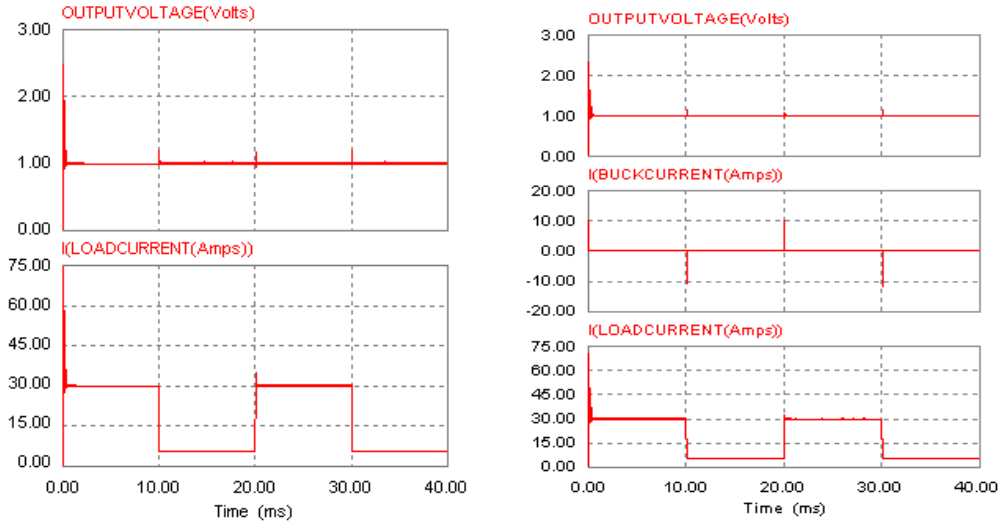


Fig. 15. Output voltage, buck current and load current without and with buck converter (parallel), for asymmetrical HB with current doubler

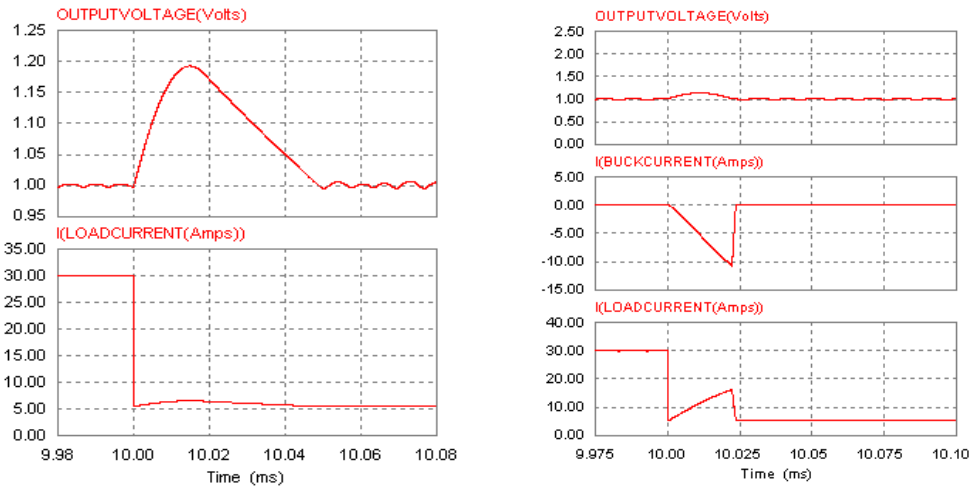


Fig. 16. Output voltage, buck current and load current for step-down load transient without and with buck converter (parallel), for asymmetrical HB with current doubler

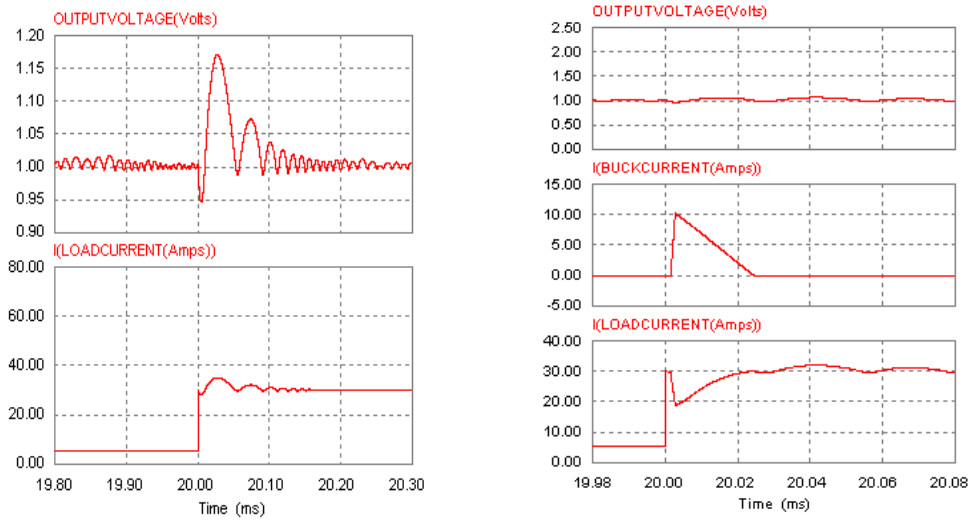


Fig. 17. Output voltage, buck current and load current for step-up load transient without and with buck converter (parallel), for asymmetrical HB with current doubler

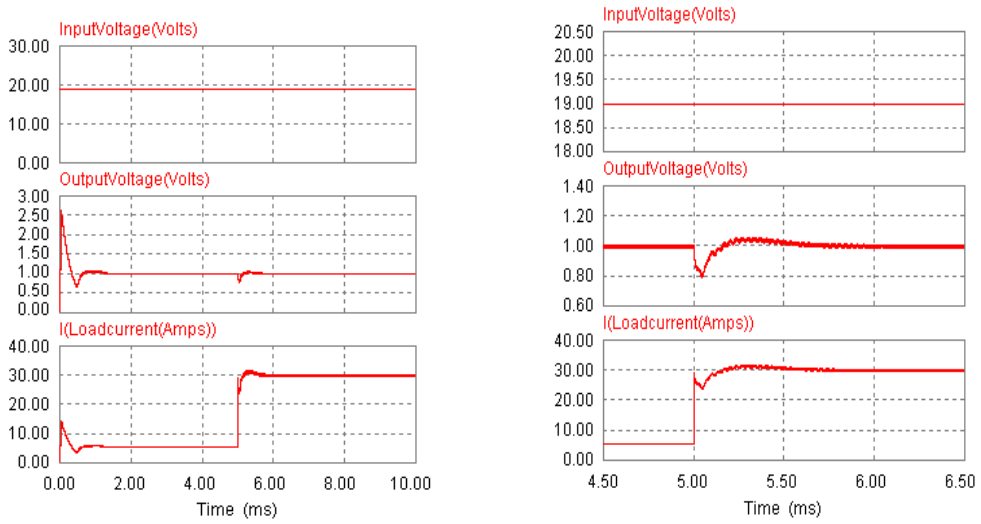


Fig. 18. Output voltage and load current of QBC with ACM controller

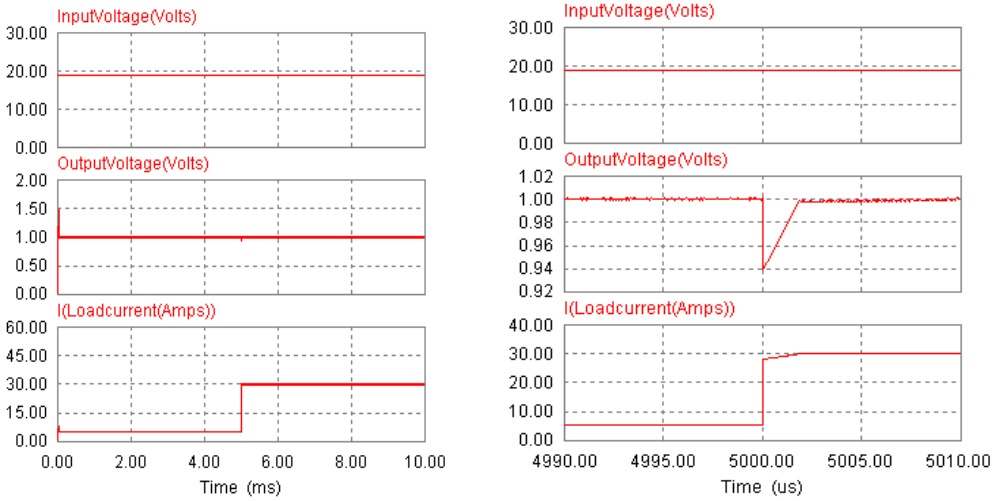


Fig. 19. Output voltage and load current of QBC with sliding-mode (SM) current controller

**Table 1.** Steady state as well as Dynamic performance and estimated cost comparison of different topologies

| Converter topology | Transient voltage deviation (TVD) % | Transient settling time (TST) | Steady state voltage ripple (SSVR) | Efficiency comparison using Power Diodes, Schottky Diodes & SR | | Estimated Cost of Hardware Prototype ($) |
|---|---|---|---|---|---|---|
| 4-phase interleaved synchronous buck converter with voltage-mode hysteretic control | 9.0%(fall) | 1.30msec | 0.001V | Power Diodes | 50.22% | $23.695 |
| | | | | Schottky Diodes (SDs) | 70.59% | $27.695 |
| | | | | MOSFETs & SDs | 91.79% | $34.499 |
| 4-phase non-coupled inductor buck converter with voltage-mode (VM) controller | 14.0%(fall) | 0.40msec | 0.01V | Inherent Body Diodes(IBD) | 95.21% | $23.717 |
| | | | | Schottky Diode in parallel with IBD | 95.69% | $31.717 |
| 4-phase coupled-inductor buck converter with voltage-mode (VM) controller | 18.0%(fall) | 0.05msec | 0.001V | Inherent Body Diodes(IBD) | 97.34% | $22.557 |
| | | | | Schottky Diode in parallel with IBD | 97.56% | $30.557 |
| Asymmetrical HB with CD for step-down load transient (Without buck) | 20%(rise) | 0.06msec | 0.01V | Power Diodes | 44.32% | $21.391 |
| | | | | Schottky Diodes (SDs) | 60.82% | $25.391 |
| | | | | MOSFETs & SDs | 86.92% | $30.111 |
| Asymmetrical HB with CD for step-down load transient (With parallel buck) | 10%(rise) | 0.025msec | 0.01V | Power Diodes | 43.82% | $24.372 |
| | | | | Schottky Diodes (SDs) | 60.32% | $29.372 |
| | | | | MOSFETs & SDs | 86.42% | $35.733 |
| Asymmetrical HB with CD for step-up load transient (Without buck) | 5.0%(fall) | 0.30msec | 0.01V | Power Diodes | 44.32% | $21.391 |
| | | | | Schottky Diodes (SDs) | 60.82% | $25.391 |
| | | | | MOSFETs & SDs | 86.92% | $30.111 |
| Asymmetrical HB with CD for step-up load transient (With parallel buck) | 5.0%((fall) | 0.02msec | 0.01V | Power Diodes | 43.82% | $24.372 |
| | | | | Schottky Diodes (SDs) | 60.32% | $29.372 |
| | | | | MOSFETs & SDs | 86.42% | $35.733 |
| QBC with ACM controller | 20.0%(fall) | 0.60msec | 0.01V | Power Diodes | 51.07% | $23.118 |
| | | | | Schottky Diodes (SDs) | 66.82% | $26.118 |
| | | | | MOSFETs & SDs | 84.20% | $28.008 |
| QBC with SM current controller | 6.0%(fall) | 5.00µsec | 0.001V | Power Diodes | 48.23% | $22.118 |
| | | | | Schottky Diodes (SDs) | 63.98% | $25.118 |
| | | | | MOSFETs & SDs | 83.10% | $27.008 |

Table 1 shows the performance comparison of different topologies in terms of TVD, TST, SSVR, efficiency and the estimated cost. The estimated cost for implementing hard-ware prototype is calculated for a purchase of 1000 units at bulk. The SR based QBC topology with sliding-mode (SM) current control strategy is less expensive ($27.008) and also the dynamic performance is good compared to the other topologies with a TVD of 6% and reaches steady state with a transient settling time (TST) of 5.0µsec. The SR based asymmetrical HB with current doubler costs more ($35.733) compared to the other topologies. The efficiency is higher (97.56%) with 4-phase coupled inductor and lower (83.10%) in case of QBC with sliding-mode (SM) current controller. The steady state voltage ripple is almost comparable in all the above topologies.

## 4. Conclusions

This paper presented a broad review on dc-dc converter topologies like multi-phase synchronous buck, multiphase non-coupled and coupled-inductor buck converters, asymmetrical half-bridge converter with current doubler and the quadratic buck converter (QBC) for lap-top computer Voltage Regulator Module (VRM) applications. The simulation results of each topology are presented and 4-phase coupled-inductor buck converter with synchronous rectification gives highest efficiency (97.56%) compared to the other topologies. But the dynamic performance is not satisfactory with a TVD of 18.08% and TST of 50µsec. In VRM applications where fast load-transitions are required inaddition to the reduced cost, the QBC with sliding-mode (SM) current controller is preferable due to good dynamic performance compared to all other topologies, the TVD is 6% of rated voltage and a transient settling time (TST) of 5.0µsec. Eventhough the control parameter tuning is simple with SM current control, the ideal robustness is not possible because of the requirement of infinite switching frequency of the power converter.

## References


[1] Moore, G.: *Cramming more components onto integrated circuits.* In: Journal of Electronics, Vol. 38, No. 8, April 1965, pp. 16.

[2] Standford, E.: *Power technology roadmap for microprocessor voltage regulators.* In: Proc. PSMA, February 2003.

[3] Intel document.: *Moore's Law: Made real by Intel Innovation*. (At http://www.intel.com/technology/timeline.pdf)

[4] Huy Nguyen.: *Design, Analysis and Implementation of Multiphase Synchronous Buck DC-DC Converter for Transportable Processor*. In: Ph.d thesis, 2004.

[5] Orabi, M., Shawky, A.: *Proposed Switching Losses Model for Integrated Point-of-Load Synchronous Buck Converters*. In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp. 5136 - 5150.

[6] Yong-Seong Roh., Young-jin Moon., Jeongpyo Park., Min-Gyu Jeong., Changsik Yoo.: *A Multiphase Synchronous Buck Converter With a Fully Integrated Current Balancing Scheme*. In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp. 5159-5169.

[7] Svikovic, V., Cortes, J.J., Alou, P., Oliver, J.A., Garcia, O., Cobos, J.A.: *Multiphase Current-Controlled Buck Converter With Energy Recycling Output Impedance Correction Circuit (OICC)*. In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp. 5207-5222.

[8] Jia wei., Lee, F.C.: *Two-Stage Voltage Regulator for Laptop Computer CPUs and the corresponding Advanced Control Schemes to Improve Light-Load performance*. In: Proc. IEEE 2004, pp. 1294-1300.

[9] Kaiwei Yao., Lee, F.C., Ming Xu., Mao Ye.: *Tapped-Inductor Buck Converter for High-Step Down DC-DC Conversion*. In: IEEE transaction on power electronics, Vol. 20, No. 4, July 2005, pp. 775 -780.

[10] Kaiwei Yao., Lee, F.C., Meng, Y., Wei, J.: *Tapped buck converter with a lossless clamp circuit.* IEEE APEC'02.

[11] Xu, P., Wei, J., Lee, F.C.: *The active-clamp couple-buck converter - A novel high efficiency voltage regulator modules.* In: IEEE APEC'01, pp. 252 -257.

[12] Guo, J.: *High performance forward converter in non-isolated configurations*. In: IEEE, INTELEC'03, pp. 761-765.

[13] Xu, P., Wei, J., Lee, F.C.: *A high efficiency topology for 12V VRM-push-pull buck and its integrated magnetics implementation*. In: IEEE, APEC'02, pp. 679-685.

[14] Minjae Kim., Sewan Choi.: *A Fully Soft-Switched Single Switch Isolated DC-DC Converter*. In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp. 4883-4890.

[15] Xinke Wu., Hui Chen., Junming Zhang., Fangzheng Peng., Zhaoming Qian.: *Interleaved Phase-Shift Full-Bridge Converter With Transformer Winding Series–Parallel Autoregulated (SPAR) Current Doubler Rectifier.* In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp. 4864 - 4873.

[16] Zhihua Yang., Sheng Ye., Yanfei Liu.: *A Novel Non-Isolated Half Bridge DC-DC converter*. In: IEEE 2005, pp. 301-307.

[17] Jae-Bum Lee., Jae-Kuk Kim., Jae-Hyun Kim., Jae-Il Baek., Gun-Woo Moon.: *A High-Efficiency PFM Half-Bridge Converter Utilizing a Half-Bridge LLC Converter Under Light Load Conditions*. In: IEEE trans. Power Electronics, Vol. 30, No. 9, 2015, pp.

4931- 4942.

[18] Chakraborty, S., Chattopadhyay, S.: *An improved asymmetric half-bridge converter with zero DC offset of magnetizing current*. In: IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 1- 8.

[19] Law, Y.Y., Kong, J.H., Liu, J.C.P., Poon, N.K., Pong, M.H.: *Comparison of three topologies for VRM fast transient application.* IEEE APEC'02 Vol. 1, pp. 210-215.

[20] Pit-leong, W., Peng, X., Yang, P., Lee, F.C.: *Performance improvements of interleaving VRMs with coupling inductors*. IEEE Trans. Power Electron., 2001, Vol. 16, No. 4, pp. 499-507.

[21] Amoroso, L., Donati, M., Zhou, X., Lee, F.C.: *Single shot transient suppressor for high current high slew rate Microprocessor*. Proc. IEEE APEC, 1999, pp. 284-288.

[22] Wang, X., Li, Q., Issab.: *Transient response improvement in isolated DC-DC converter with current injection circuit.* Proc. IEEE APEC, 2005, Vol. 2, pp. 706-710.

[23] Wang, X., Huaz., Majd, B., Issab., Chickamenahalli, S.A., Stanford, E.: *Active transient voltage compensator design for VR load line improvement*. Proc. IEEE APEC, 2006, pp. 59-64.

[24] Abu-Qahouq, J. A., Pongratananukul, N. I., Batarseh., Kasparis, T.: *Multiphase Voltage-Mode Hysteretic Controlled VRM With DSP Control and Novel Current Sharing*. In: Proc. IEEE 2002, pp. 663-669.

[25] Yan Dong.: *Investigation of Multiphase Coupled-Inductor Buck Converters in Point-of-Load Applications*. In: Ph.d thesis, 2009.

[26] Bo Yang.: *State of the Art Topologies and Improvements*. In: Ph.d thesis, 2003.

[27] Panguloori, R.B., Debaprasad, K., Amit, P., Capodivacca, G.: *High Performance Voltage Regulator for High Step-Down DC-DC Conversion*. In: IEEE Industrial Electronics Conference, 2008, pp.761-765.

[28] Panguloori, R.B., Debaprasad, K., Amit, P.: *Design and performance studies of a hybrid voltage regulator with improved energy efficiency*. In: IET Power Electron., Vol. 3, No. 6, 2010, pp. 915-924.

[29] Sondeep Bassan., Gerry Moschopoulos.: *Properties and applications of quadratic converters*. In: IEEE Canada Electrical Power Conference, Oct.2007, pp.123-127.

[30] Carbajal Gutierrez, E. E., Morales Saldana, J. A., Leyva Ramos, J.: *Average Current-mode control for a quadratic buck converter*. In: Proc. IEEE Power Electron. Spec. Conf., 2005, pp. 2146-2150.

[31] Jorge Alberto, M.S., Rodrigo, L.P., Elvia, P.H.: *Parameters selection criteria of proportional-integral controller for a quadratic buck converter*. In: IET Power Electronics, Vol. 7, No. 6, 2014, pp. 1527-1535.

[32] Ayachit, A., Kazirnierczuk, M.K.: *Power Losses and Efficiency Analysis of the Quadratic Buck Converter in CCM*. In: Proc. IEEE Midwest Symp. Circuits Syst. College Station, TX, 2014, pp. 463-66.

[33] Yadlapalli, R.T., Kotapati, A.: *A fast-response sliding-mode controller for quadratic buck converter*. In: Int. J. Power Electronics, Vol. 6, No. 2, 2014, pp.103-130.

[34] Yadlapalli, R.T., Kotapati, A.: *An efficient sliding-mode current controller with reduced flickering for quadratic buck converter used as LED lamp driver.* In: Int. J. Power Electronics, Vol. 6, No. 4, 2014, pp. 345-375.