FIELD PROGRAMMABLE GATE ARRAY BASED THREE-PHASE CASCADED MULTILEVEL VOLTAGE SOURCE INVERTER

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Abstract: This paper presents a Field Programmable Gate Array (FPGA) controller based three-phase conventional and cascaded multilevel voltage source inverter (VSI) fed adjustable speed induction motor drive applications. This inverter should maintain the variation of both voltages and frequency simultaneously; it keeps their V/F ratio constant for control of speed. In this investigation, a simple novel control circuit is adopted using FPGA devices for the hardware implementation. It can be accommodated in a single chip that provides high computation speed and accurate control signals for higher output voltages with less harmonic content. VHDL language is used to model the inverter switching strategies. The proposed controller generates 6-control signals to conventional inverter and 36-control signals to cascaded inverter switches for 3-level and 7- level output voltage respectively. Matlab/System generator and XILINX tools are used with hardware-co-simulation to synthesize the architecture and the obtained architecture is embedded in FPGA.

Key words: *cascaded multilevel voltage source inverter, Sinusoidal PWM, Field Programmable Gate Array (FPGA), VHDL*

1. Introduction.

Cascaded multilevel three-phase voltage source inverters have turned out to be greater research attention in the past few years [1]. Sinusoidal pulse width modulation technique is widely used in power electronics to optimize the power system controller and it gives dc-input voltage to symmetrical ac-output voltage of desired magnitude and frequency [2]. These SPWM based cascaded power converters provide advantages such as, high power quality waveforms, low switching losses, and high-voltage capability [3]. The literature covered three main types of transform less multilevel inverter topologies; flying capacitor inverter, diode clamped inverter and the cascaded H-bridge inverter. Among these inverter topologies, the flying capacitor inverter is difficult to be realized because each capacitor must be charged with different voltages as the voltage level increases [4-5]. Moreover, the clamped inverter also known as a neutral clamped converter is difficult to be expanded to multilevel because of the natural problem of the DC link voltage unbalancing. The cascaded inverter has the disadvantage of requiring a separate dc sources, yet these cascaded inverter has been widely found applications in the field of HVDC, high-power motor drive, adjustable speed drive (ASDs), UPS and active power filter and so on [6-7].

This paper focus on SPWM based conventional and cascaded multilevel inverter fed adjustable speed of induction motor drives applications [8-9]. Adjustable speed AC machine system is equipped with an adjustable frequency drive that is a power electronic device for speed control of an electric machine. It controls the speed of the electric machine by converting the fixed voltage and frequency of the grid to adjustable values as required. The speed of an induction motor is controlled by varying the frequency of the power applied to its stator windings [10-11]. In order to obtain substantially full-load torque capability at all operating speeds it is also necessary to be able to achieve maximum air-gap flux in the motor. In a voltage-source inverter drive, flux is often held near maximum at all times by maintaining a constant motor voltage-to-motor speed ratio. The cascaded multilevel inverter fed ASDs has the features of higher speeds with a low switching frequency, which offers high conversion efficiency and cost criteria [12-13].

In recent years digital control techniques are becoming the most widespread resolution in modern power electronics application [14]. The microprocessors, DSP processor and application specific integrated circuits (ASIC) are responsible for better performances of the power converters. Yet the design of digitally controlled power electronics is affected by several problems, such as sampling rate software portability, re-usability, high level language problem, peripheral devices and register settings specific for each microprocessor. A change of the microprocessor for better performance requires a huge revision of the project. Such an operation is time consuming, expensive, sometimes unsuccessful and the expertise gained with a specific system could not be

useful for different devices [15]. These problems can be mitigated by Field Programmable Gate Array circuits (FPGA). It does eliminate the code portability trouble as VHDL hardware description language and several development tools are almost device independent. Nowadays FPGA are becoming popular in power electronics applications due to high performance, fast time-to-market, low power logic devices and production cost [16].

In this investigation we propose a novel SPWM based FPGA control algorithm for conventional and cascaded multilevel voltage source inverter for adjustable speed of induction motor drives applications. The proposed controller design is simulated and compilation portion is tested successfully through the Spartan-3E FPGA device in real time environment. The order of harmonics with respect to amplitude and the total harmonic distortion (THD) of currents and voltages are measured and compared both conventional and cascaded inverter. This FPGA controller algorithm has reduced harmonic distortion.

2. PWM-VSI Topology

This section describes the operating principles of the three-phase conventional and cascaded multilevel voltage source inverter.

2.1. Conventional PWM-VSI inverter:

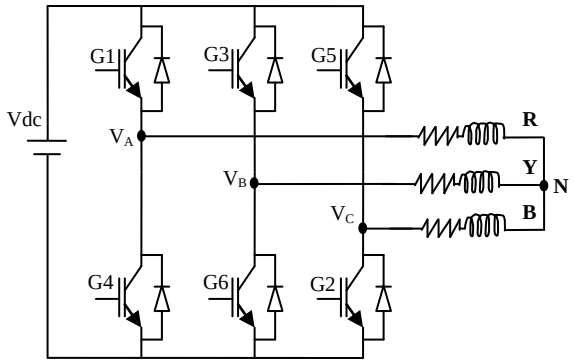

Fig. 1 Conventional voltage source inverter

The inverter is fed by a dc voltage source and has three phase legs (labeled V_A, V_B, and V_C). Each leg is having two transistor switches with two anti parallel freewheeling diodes and is connected with RL loads instead of induction motor as shown in Fig. 1. This section describes about the operating principles of the conventional 3-phase voltage source inverter. The IGBT switches of the inverter are controlled based on digitized sinusoidal pulse width modulation techniques. The digitized SPWM based control modulation index is obtained from the comparison of a digitized reference sinusoidal signal and digitized carrier saw-tooth signals. The reference sinusoidal signal (f_r) provides the desired fundamental frequency of the inverter output voltage and the carrier saw-tooth signals (f_c) gives the switching frequency of the inverter. The modulation frequency ratio (m_f) derived as $m_f = f_c / f_r$. The magnitude of the saw-tooth signals (V_c) is held fix and amplitude of the inverter output voltages is controlled by adjusting the amplitude of the reference sinusoidal control voltages (V_r). The amplitude modulation ratio (m_c) is defined as $m_c = V_r / V_c$. The ratio of modulation index controls the harmonic content of the output voltage and is proportional to the magnitude of fundamental component. The voltage and current output of the three phase voltage source inverter are controlled by changing the possible switching states. The 6-switching pulses are generated from the proposed SPWM based FPGA controller. The transistor pair in each arm G1-G2, G3-G4 and G5-G6 of the six-switching pulses is turned on with a time interval of 180 degree. It means that G1 conduct for 180 degree and G2 for next 180 degree of a cycle. The switches in the upper group G1, G2, G3 conduct at an interval of 120 degree. It implies that if G1 is fired at $\omega t = 0^0$ then G3 must fired at $\omega t = 120^0$ and G5 at $\omega t = 240^0$ for lower switches. By controlling the switches in this manner, the line-line inverter output voltages become AC-power with a fundamental frequency corresponding to the frequency of the sinusoidal control voltage. The three-possible cycles to outputs are $Vdc, 0 \; and \; -Vdc$ voltage levels. Finally, the output of the inverter is fed to an induction motor.

2.2. Cascaded multilevel voltage source inverter

The three single-phase cascaded inverter can be connected in either wye or delta configuration for a three-phase system. Fig. 2 illustrates the schematic diagram of wye-connected seven-level cascaded voltage source inverter structure. Each separate dc source is connected to an every single-phase H-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}, 0 \; and \; -V_{dc}$ by connecting the dc source to the ac-output by different combinations of the four switches $G1, G2, G3 \; and \; G4$. To obtain $+V_{dc}$, switches $G1 \; and \; G4$ are turned ON, whereas $-V_{dc}$ can

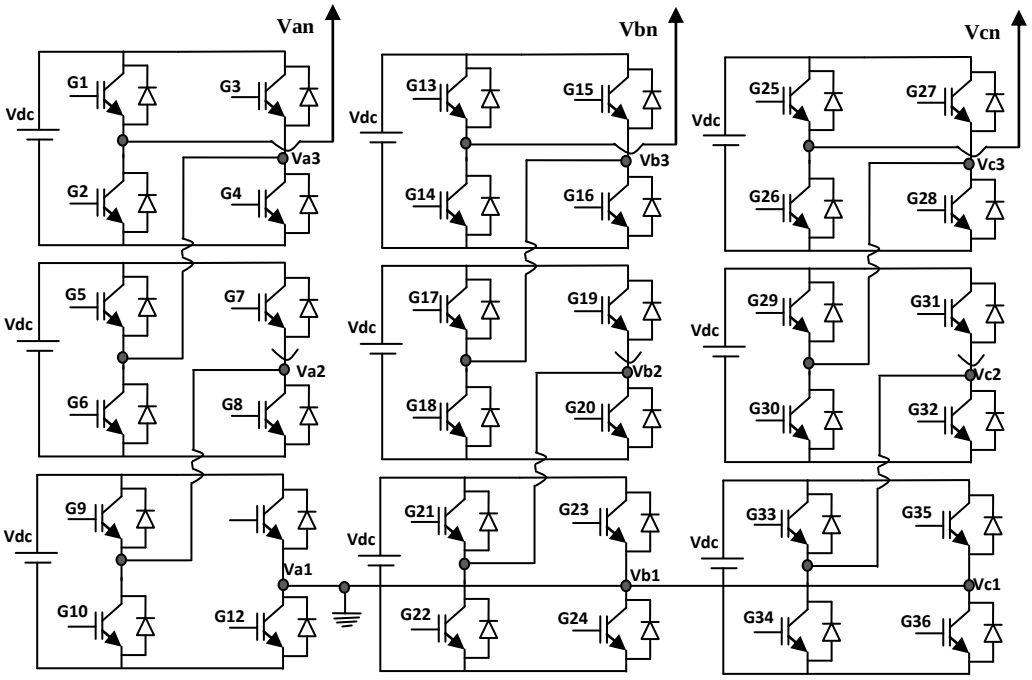

Fig. 2 Cascaded multilevel three phase voltage source inverter

be obtained by turning ON switches $G2$ *and* $G3$. By turning ON $G1$ *and* $G2$ or $G3$ *and* $G4$ the output voltage is 0. Similarly, the ac-outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Van is voltage of phase A, which is the sum of Va1, Va2, and Va3. The same estimate is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phases with delaying 0, 120, and 240 electrical degrees for phase A, B, and C, respectively

The proposed sinusoidal pulse width modulation based FPGA controller to generate 36-channel switching pulses to drive the cascaded multilevel inverter. The seven-possible cycle outputs are $3Vdc$, $2Vdc$, Vdc, 0, $-Vdc$, $-2Vdc$ and $-3Vdc$ voltage levels. The output of the inverter is fed to the induction motor. The maximum number of line voltage levels is $2m-1$, where m the number of phase voltage levels is. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The seven-level cascaded inverter can synthesize up to thirteen-level line voltage. The order of harmonics and total harmonic distortion (THD) is measured and verified with respect to the fundamental frequency. This proposed SPWM controller is tested for real time hardware validation in Xilinx/Spartan3e FPGA device through hardware-co-simulation using system generator.

3. Proposed FPGA based SPWM Controller

The block diagram of proposed FPGA controller based on conventional and cascaded multilevel inverter fed adjustable speed to drive induction motor is shown in Fig. 3. The required speed rpm (revolution per minutes) value is applied to the system, whose analog value is converted to digital fixed binary numbers for digital FPGA design controller. The digitized reference speed of 1500 rpm is multiplied with gain 1.666 for setting the amplitude 2500 V and performs with accumulator operation for setting the frequency range simultaneously. The 16-bit up-counter compared with 16-bit constant value for generating pulse signal to the enable port of 16-bit accumulator. The result of accumulator is generating sawtooth frequency and it is divided by 8-bit shifter to recover the accumulator reset port through feedback loop connection. This feedback loop makes the amplitude and frequency ratio constant. The frequency range is directly committed with 14-bit ROM device. This will generate sine signals of same phase and out of phase (180^0 phase shift) as two reference signals. To set the V/F ratio constant the setting amplitude is added with the reference signals. This V/F ratio controls the

output voltage of the conventional and cascaded multilevel voltage source inverter.

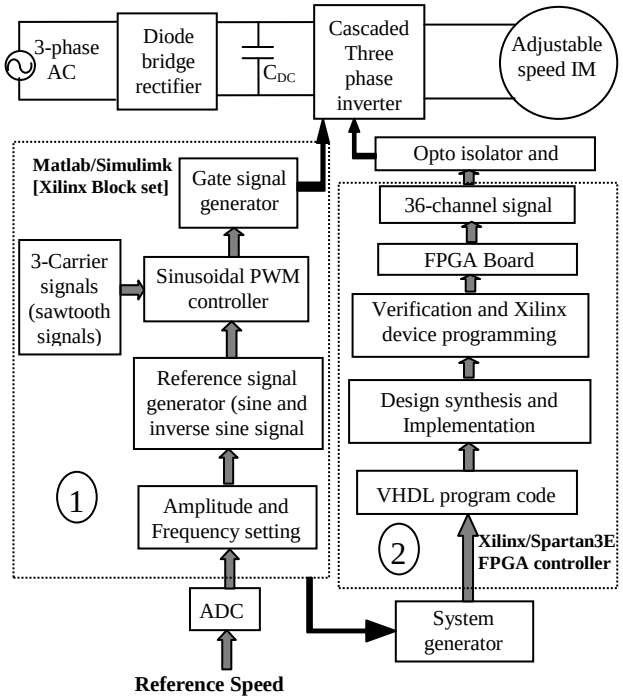

Fig. 3 Proposed block diagram of FPGA based cascaded inverter fed ASD

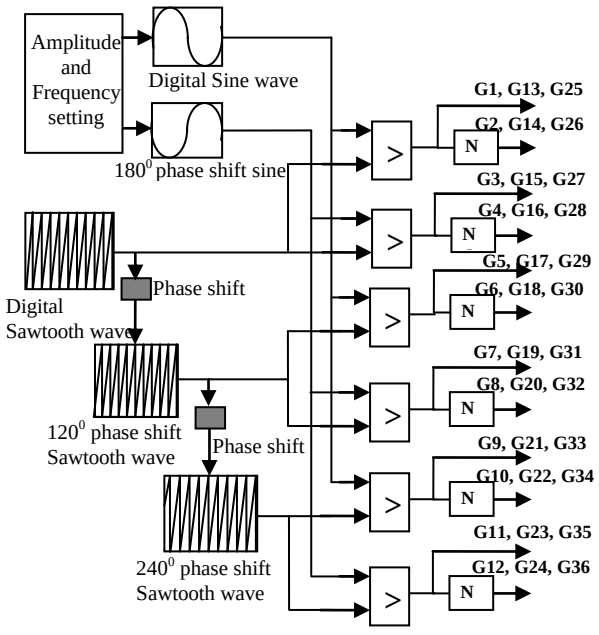

Fig. 4 System design using xilinx blockset/Matlab

The three carrier signals (sawtooth waves) are generated using up-counter design. The first sawtooth carrier signal is generated from 20-bit up-counter. These output signals phase shifted by 120^0 for second sawtooth carrier signals and 240^0 phase shift for third sawtooth carrier signals respectively. The two reference signals, sine and 180^0 phase shift sine signal compared with three sawtooth carrier waves for generating 6-primary signals, as shown in Fig. 4. The widths of the pulses depend upon the amplitude of reference sine signals. The ratio of reference and carrier amplitude is called modulation index which controls the output voltage of the inverter. This works as a sinusoidal PWM controller technique, so the reference sine waves of frequency and amplitude can easily adjust and vary the modulation index. The distribution unit of NOT gates deal with the 6- primary signals (produced from reference and carrier signals comparator) and it generates the 36-gate pulses (G1 to G36) for drive the cascaded multilevel inverter. The gate pulses G1, G2, G4, G4, G5 and G6 are used to drive the conventional inverter. The digital controller can be tested and implemented to FPGA hardware in two different ways using system generator (1) Hardware-co-simulation and (2) Xilinx ISE-iMPACT.

3.1. Hardware-co-simulation

System generator with simulink provides an environment which can be interfaced with Xilinx/Spartan3e FPGA device to run a design [14]. The compilation target automatically creates a bit stream file and dumps it into FPGA kit. After the proposed controller design is being simulated, the compilation portion is tested successfully in FPGA through the JTAG connection in real time environment.

3.2. ISE-iMPACT

The VHDL program code is generated from the system generator after simulation and verification of the control design. The VHDL program is synthesized using Xilinx-ISE 10.1 software [16]. The ISE^{TM} (Integrated Software Environment) based FPGA design flow comprises the following steps:
1) Design entry – it assign constraints such as timing, pin location, area constraints and user constraints (UCF) file. 2) Design synthesis- Synthesize the project design. 3) Design implementation- Implementation of the design includes Translate, Map, Place and Route. 4) Design verification- It includes both functional verification (also known as RTL simulation) and timing verification. 5) Xilinx® device programming-create a programming BIT file, use iMPACT to download it to target device XILINX/SPARTAN-3E with a programming cable.

Once the program is dump into FPGA kit, FPGA acts as a Sinusoidal PWM controller and generate gate drive signals. These signals are connected to optoisolator circuit for preventing the ground sharing between the FPGA chip and H-bridge power module. The output of optoisolator is connected through driver to each switching devices for controlling the PWM single phase inverter.

5. Results and Analysis

The proposed sinusoidal PWM based conventional and cascaded multilevel three phase inverter is simulated for variable speed drive applications by using Matlab/Simulink and XILINX ISE tools. The Simulink/Xilinx Block set is a powerful graphical modeling system which allows digital complex systems to be designed using a block diagram methodology. These digitized systems of the block modeling can generate VHDL code by using system generator. The VHDL program is verified and synthesized using Xilinx-ISE 10.1; then bit stream file is generated that implements the controller into targeted Spartan3e FPGA board. The system is investigated by resistive and inductive (RL-load) loads instead of induction motor.

The desired reference speed rms value is converted to digital fixed point value for digital-design. The discrete reference value set the amplitude and the frequency according to voltage and frequency ratio. The amplitude and frequency with 14-bit ROM device are generated in two reference sinusoidal signals. These maintain the voltage to frequency ratio constant by controlling the output voltage of the cascaded inverter. Fig. 5 (a) shows the sinusoidal wave and 180^0 phase shift sinusoidal wave (inverse sinusoidal wave) as a reference signals.

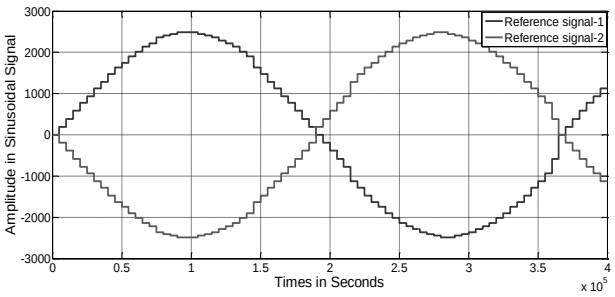

Fig. 5 (a) Reference sinusoidal signal

The three carrier signals (such as sawtooth waves) are generated using an up-counter design. The first sawtooth carrier signal is generated from 20-bit up-counter and these signals phase are shifted to 120^0 for second sawtooth carrier signals and 240^0 for third sawtooth carrier signals. Fig. 5 (b) shows each sawtooth wave starts from different amplitude with 120^0 phase shift. This sawtooth wave amplitude is -2500 V, -800 V, and +900 V to +2500 V.

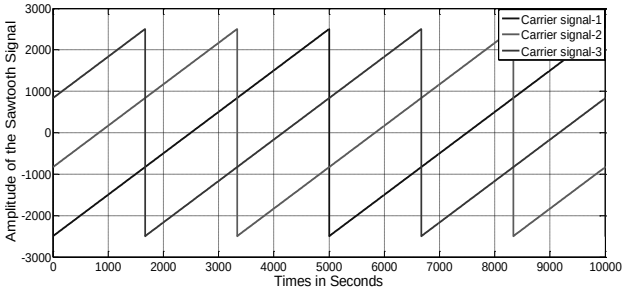

Fig. 5 (b) Three carrier sawtooth signals

The first reference sinusoidal signal is compared with the three sawtooth carrier signals, similarly the second 180^0 phase shift reference sinusoidal signal is also compared with the same three sawtooth carrier signals. Therefore, two sinusoidal signals are separately compared with three sawtooth signals to generate 6-gate signals. The distribution unit of NOT gates deals with the 6- signals and generates 12-gate signals for driving the IGBTs switches. The Very high speed integrated circuits Hardware Description Language (VHDL) can be used to model a digital system at many levels of abstraction, ranging from the algorithmic level to gate level with high degree of complexity. Fig 6 (a) shows the decimal value, bit waveforms of ADC reference speed value, amplitude and frequency. It also shows sinusoidal wave, 180^0 phase shift sinusoidal wave (inverse sinusoidal) for reference signals, up-counter, 120^0 phase shift up-counter and 240^0 phase shift up-counter for carrier sawtooth signals.

The 6-channel gate control pulses are generated from the comparison of two reference sine wave signals with three carrier sawtooth signals as shown in Fig. 6 (b). The VHDL program is generated from the system generator using simulink platform. According to the clock pulse, the 6-switching signals are used to drive the conventional 3-phase inverter for 3-level output voltage. The 36-channel gate control pulses are generated from the comparison of two reference sine signals with three carrier sawtooth signals as shown in Fig. 6 (c). According to the clock pulse, the 36-switching signals are used to drive the cascaded multilevel three phase voltage source inverter for 7-level output voltage.

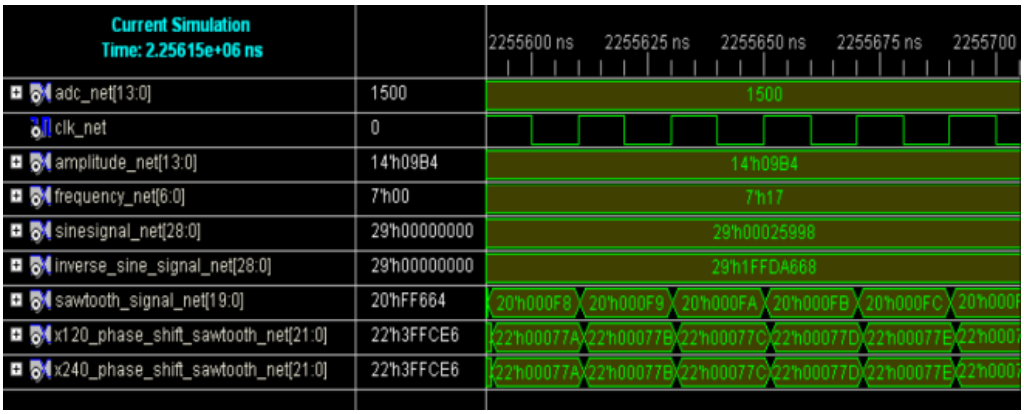

Fig. 6 (a) VHDL simulation for proposed system design

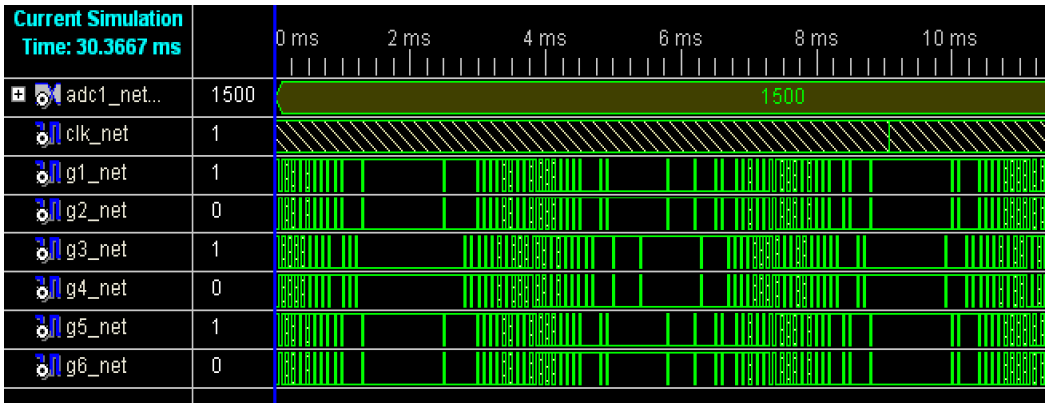

Fig. 6 (b) Conventional inverter switching pulses

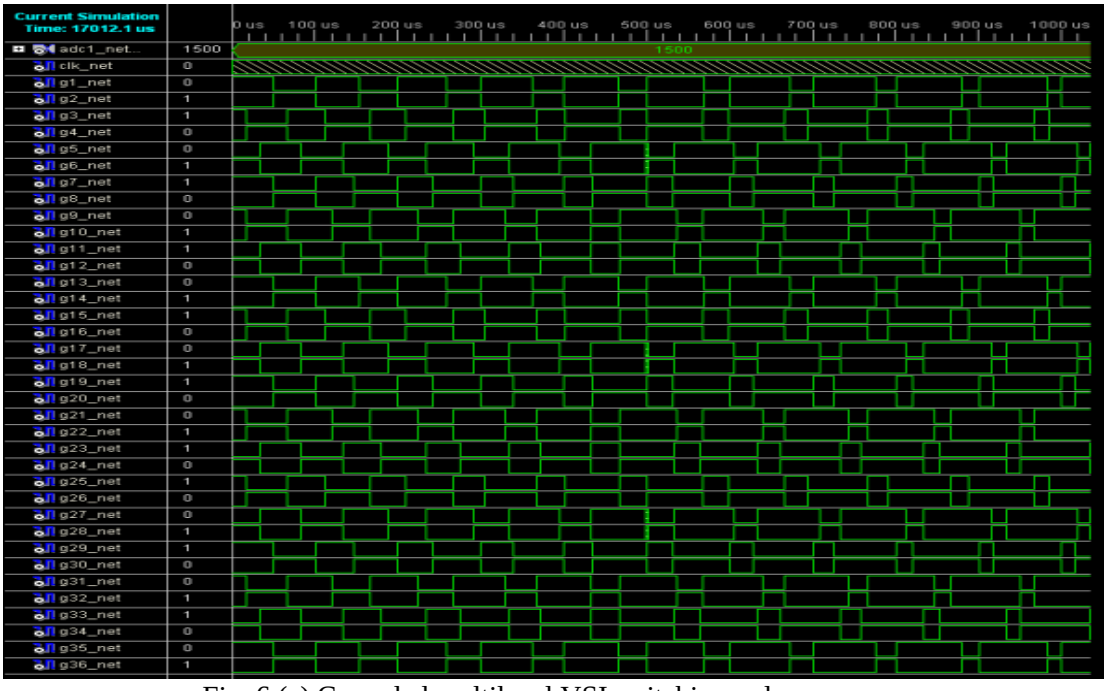

Fig. 6 (c) Cascaded multilevel VSI switching pulses

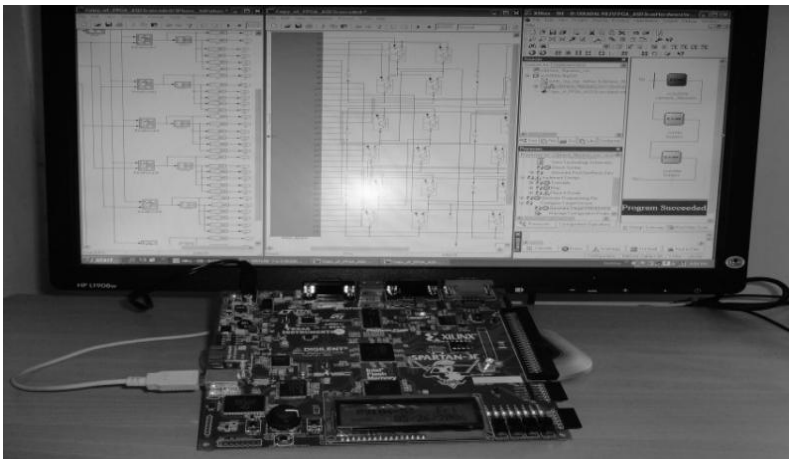

Fig. 7 Experimental setup using Hardware-co-simulation

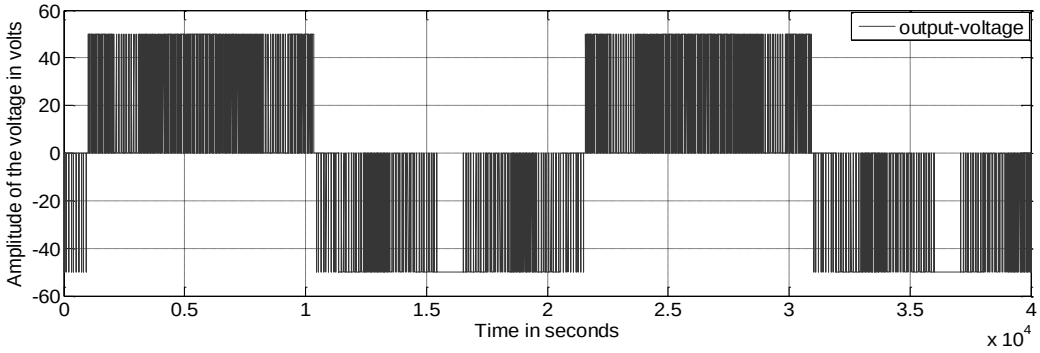

Fig. 8 (a) Output voltage of conventional 3-phase inverter

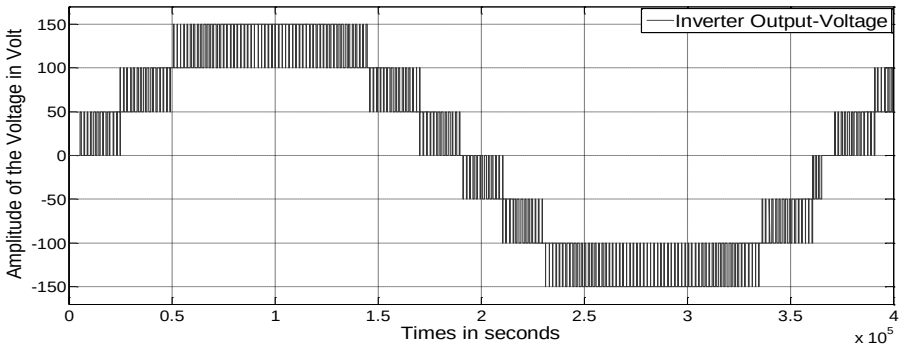

Fig. 8 (b) Output voltage of cascaded multilevel 3-phase inverter

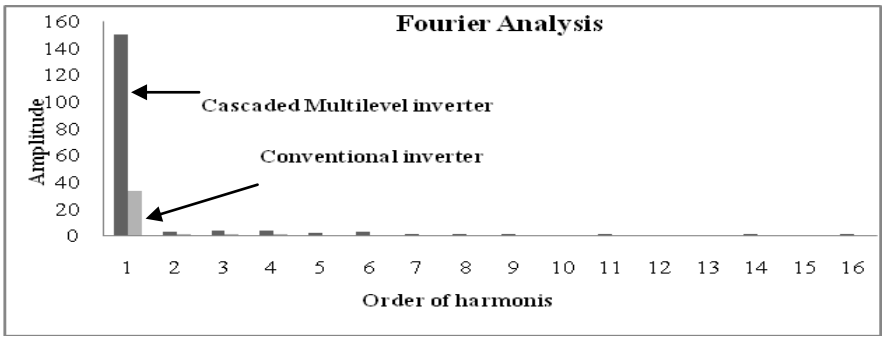

Fig. 9 order of harmonic measured with respect to the magnitude

The experimental setup is built in conjunction with hardware-co-simulation platform that is shown in Fig. 7. The system generator is provides the interface with Xilinx-Spartan3E board in two ways; (1) direct interface through JTAG chain, (2) Xilinx-iMPACT interface through USB cable. The JTAG options choose the boundary scan and IR length that is used to program the FPGA. The USB cable is able to program the FPGA with 12 MHz speed. The compilation target automatically creates a bit stream file and dumps it to FPGA board. This system clock frequency for hardware co-simulation is set at 50 MHz at pin location C9 of the FPGA board. The proposed controller design is simulated and compilation portion is tested successfully through the FPGA kit in real time environment.

The proposed sinusoidal PWM controller design is implemented to Spartan3e device FPGA board and tested using hardware-co-simulation. The FPGA board is generating 6-channel gate pulses to drive the conventional 3-phase voltage source inverter switches that produce 3-level output voltage as shown in Fig. 8 (a). As shown in Fig. 8 (b) the FPGA board is generating 36-channel gate pulses that are used to drive the cascaded multilevel voltage source inverter switches and produce 7-level output voltage. The output voltage levels are $3Vdc$, $2Vdc$, Vdc , 0 , $-Vdc$, $-2Vdc$ and $-3Vdc$. This proposed controller with suitable cascaded inverter topology claim less total harmonic distortion

The Fourier analysis of the source current is done to find magnitudes of different harmonic components. The conventional and cascaded multilevel inverter output voltage harmonics are plotted in Fig. 9.

The conventional and cascaded multilevel voltage source inverter of the total harmonic distortion (THD) is calculated. The output current and voltage of the THD is measured as shown in table 1.

Table 1 THD measured of the conventional and cascaded 3-phase VSI

THD	Conventional 3-phase VSI	Cascaded multilevel 3-phase VSI
Voltage	52.82%	19.31%
Current	11.62%	03.41%

5. Conclusions

The sinusoidal pulse width modulation based FPGA controller provides switching patterns that are adopted and applied to the conventional and cascaded multilevel inverter to generate 3-level and 7-level output voltages respectively. This controller design is simulated and compilation portion is tested successfully through the FPGA hardware implementation in real time environment using hardware-co-simulation. The FPGA allows easy, fast and flexible implementation of control circuit hardware. It can effectively adjust the modulation index range for varying speed control of induction motor drives. The effective controller maintains the voltage to frequency ratio constant. The experimental and simulation results demonstrate quality voltage and current waveform shapes with fewer harmonics at the output of the inverter. These inverter topologies with proposed control circuit can be used for speed control of induction motor and other industrial applications

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