DESIGN AND IMPLEMENTATION OF QUASI RESONANT- NEGATIVE OUTPUT SUPER LIFT LUO CONVERTER

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Abstract: *This paper presents the analysis, design and voltage regulation of a Zero Voltage Switching Quasi Resonant – Negative output Super lift Luo Converter with low switching losses for aerospace applications. To increase the power packing density, a simple control method using an analog resonant controller UC3861 is used to regulate the output voltage against load variations and supply disturbances. The performance of the controller is verified by developing a prototype model of the converter and experimental results are presented. The results reveal the superiority of using a single dedicated IC for voltage regulation. Also it is observed that the converter provides maximum efficiency of 96% at full load.*

Key words: *Error Amplifier (E/A), Frequency Modulation (FM), Switched Mode Power Supply (SMPS), Under Voltage Lock Out (UVLO), UC3861 (Analog resonant controller), Zero Voltage Switching Quasi Resonant-Negative Output Super Lift Luo (ZVS QR-NOSLL) converter.*

1. Introduction

Switched mode Pulse Width Modulated (PWM) dc-dc converters play an important role in communication, automobile, computer and aerospace applications. In aerospace applications the allowable size and weight are highly restricted to accommodate greater payload. To increase the power packing density and to reduce the size and weight of the magnetic and filter components, the switching frequency of the converter has to be increased. At high frequencies, the conventional PWM switched mode converters are unsuitable as they experience high switching losses, reduced reliability, electromagnetic interference and acoustic noise. To overcome the above difficulties, Quasi-Resonant converters (QRCs) are used. High power density and improved efficiency can be obtained with these converters because the commutation takes place either under Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) [1].

Voltage Lift (VL) technique is a popular method that is widely used in electronic circuit design [2]. It has been successfully employed in buck, boost, buck boost and higher order CUK, SEPIC, double – output dc-dc converter applications in recent years. It has opened a way to design high voltage gain power converters. In these power converters, the output voltage increases in an arithmetic progression manner [3], [4],[5],[6],[7].

In Super Lift (SL) power converter, the output voltage increases stage by stage in geometric progression. It effectively enhances the voltage transfer gain in power-law. SL technique has been implemented in positive and negative output SL Luo-converters, positive output Cascade boost converter [8], [9],[10]. The analysis of SL Luo-converters with capacitor voltage drop is reported in [11].

To improve the efficiency of power dc-dc converters, it is proposed to apply ZVS /ZCS resonant switching techniques to the existing power dc-dc converters. The voltage regulation of QRCs against load variations and supply voltage fluctuations is one of the important criteria for designing high-density power supplies. In order to improve the speed of response and to achieve voltage regulation, it is necessary to have a closed-loop control system. The PID controller design for the voltage control of converters based on average modeling has been reported in [12]. An output voltage regulation of a high–efficiency, high step-up dc-dc power converter is reported in [13]. The small signal analysis and mathematical modeling of power dc-dc converters are reported in [14], [15]. The above systems are sensitive to both operating points and parameter variations. Also regulation is achieved by using analog PI controller and switching pulses are generated using analog pulse generating circuit. Moreover, a driver circuit is also used to drive the switches. In addition, separate power supplies are needed to activate the circuits. This in turn increases the size and weight of the converter. These drawbacks can be overcome by using a dedicated analog controller IC UC3861 for voltage regulation of QRCs under voltage mode control. The above controller has a built in PI controller and derives power from converter circuit itself and generates switching pulses at zero crossing instances of resonant capacitor voltage. This can increase the power packing density and efficiency of the converter. The application of analog resonant controller UC3861 to Constant Frequency – ZVS - QRC is reported in [16].

However, to the authors' knowledge, the application of analog resonant controller for the voltage control of ZVS QR-NOSLL converter has not been reported. Hence it is proposed to regulate the output voltage of ZVS QR-NOSLL converter using UC3861.Also it is proposed to verify the performance of the controller for load and supply variations.

2. Analysis of ZVS QR-NOSLL converter

The circuit diagram of ZVS QR-NOSLL converter is shown in Fig. 1. It consists of a switch S, inductor L_1, diodes D_1, D_2 and capacitors C_1,C_2 .The capacitor C_r and inductor L_r form a resonant circuit. Conduction duty ratio is K, switching frequency is f_s (period $T_s=1/f_s$) and the load is a resistive load R_0. The input voltage and current are V_{in} and I_{in}. Output voltage and current are V_0 and I_0. The voltage transfer gain is $M = V_0/V_{in}$.

To analyze the steady state behaviour of the ZVS QR-NOSLL converter operating in continuous conduction mode, the following assumptions are made:

1. Semiconductor switches are ideal, i.e. no forward voltage drop in the ON state, no leakage current in the OFF state and no time delay at both turn-ON and turn-OFF.
2. Reactive elements in the circuit are ideal.
3. Inductors L_1 and L_2 are larger than resonating inductor L_r.
4. The output capacitor C_2 and the load R_0 is a constant sink of output current I_o.

To analyze the steady state behavior of ZVS QR-NOSLL converter, each switching cycle is divided into four modes of operation. The following circuit parameters are defined for analysis.I_M, i_{Lr}, v_{c_r}, v_{L_r} and Z_0 are defined as magnetizing current, resonant inductor current, resonant capacitor voltage, resonant inductor voltage and characteristic impedance respectively. The equivalent circuit for each mode and the theoretical waveforms of resonant capacitor voltage and inductor current are shown in Fig. 2 and Fig 3. respectively.

2.1. Modes of operation

2.1.1. Mode I

This mode is valid for $t_0 \le t \le t_1$. At $t=t_0$, the switch S is turned off, under ZVS condition. During this mode, the resonant inductor current $i_{L_r}(t)$ is held constant at I_M. The current $i_{L_r}(t)$ charges C_r from 0 to V_{in}. The equivalent circuit diagram of this mode is shown in Fig. 2(a).

The resonant capacitor voltage $v_{C_r}(t)$ and inductor current $i_{L_r}(t)$ are given by

$$v_{C_r}(t) = \frac{I_M t}{C_r} \tag{1}$$

$$i_{Lr}(t) = I_M \tag{2}$$

At $t = t_1$, the resonant capacitor voltage reaches V_{in}.

The duration of this mode is given by

$$T_{d1} = \frac{C_r V_{in}}{I_M} \tag{3}$$

2.1.2. Mode II

This mode is valid for $t_1 \le t \le t_2$. During this mode as the switch S remains off, the elements L_r and C_r form a series resonant circuit and resonate with each other. The equivalent circuit diagram of this mode is shown in Fig. 2(b). As the current through L_r starts decreasing, it causes an increase in voltage across C_r. At $t = t_1^{I}$, the current $i_{L_r}(t)$ reaches to zero and $v_{C_r}(t)$ reaches the maximum value.

$$v_{C_r}(t) = V_{C_{r-peak}} = V_{in} + Z_0 I_M \tag{4}$$

$$i_{L_r}(t) = 0 \tag{5}$$

The current I_M should be sufficiently large so that $I_M Z_0 > V_{in}$ is satisfied to obtain the ZVS condition. Otherwise, the switch voltage will not come back to zero naturally, resulting in turn-on loss.

During the period $t_1^{I} \le t \le t_1^{II}$, the energy transfers from C_r back to L_r decreasing $v_{C_r}(t)$ from its maximum value to V_{in} and current $i_{L_r}(t)$ reaches the negative maximum I_M.

At $t = t_1^{II}$

$$v_{C_r}(t) = V_{in} \tag{6}$$

$$i_{L_r}(t) = -I_M \tag{7}$$

At $t = t_2$, the voltage $v_{C_r}(t)$ reaches zero, to achieve zero voltage condition for switch S.

$$v_{C_r}(t) = 0 \tag{8}$$

$$i_{L_r}(t) = -I_M \cos\alpha \tag{9}$$

$$where \alpha = \sin^{-1}\left(\frac{V_{in}}{I_M Z_0}\right)$$

Time duration for this mode is given by

$$T_{d2} = t_2 - t_1 = \left(\frac{\pi + \alpha}{\omega_0}\right) \tag{10}$$

2.1.3. Mode III

This mode is valid for $t_2 \le t \le t_3$. The switch S is closed at $t=t_2$. The current $i_{L_r}(t)$ increases linearly with a slope of V_{in} / L_r from $-I_M \cos\alpha$ to 0. The

equivalent circuit diagram of this mode is shown in Fig. 2(c). The duration of this mode is given by

$$T_{d3} = \frac{(I_M \cos\alpha)(L_r)}{V_{in}} \qquad (11)$$

2.1.4. Mode IV

This mode is valid for $t_3 \le t \le t_4$. During this mode $i_{L_r}(t)$ increases linearly from 0 to I_M. This mode continues until the switch S is opened at t = t_4 and the cycle repeats. The equivalent circuit diagram of this mode is shown in Fig. 2(d). The duration of this mode is given by

$$T_{d4} = T_s - \left(T_{d1} + T_{d2} + T_{d3}\right) \qquad (12)$$

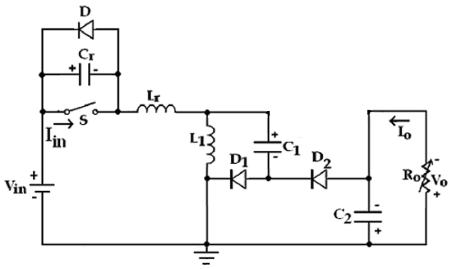
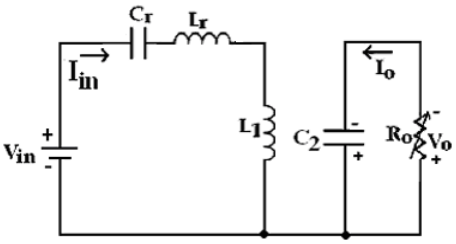
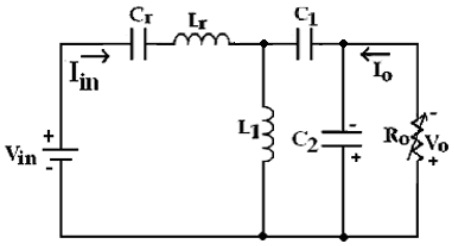


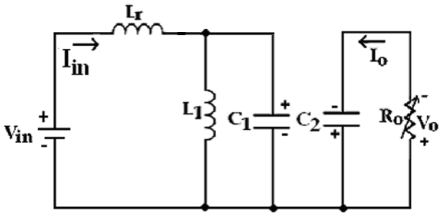
Fig. 1. Circuit diagram of ZVS QR- NOSLL Converter



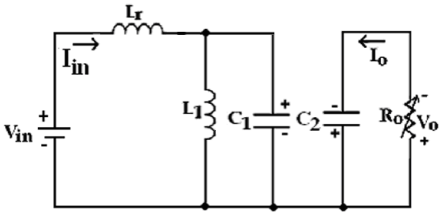
(a) Mode I ($t_0 \le t \le t_1$)



(b) Mode II ($t_1 \le t \le t_2$)



(c) Mode III ($t_2 \le t \le t_3$)



(d) Mode IV ($t_3 \le t \le t_4$)

Fig. 2. Equivalent circuit of ZVS QR-NOSLL converter in four topological modes of a switching cycle.

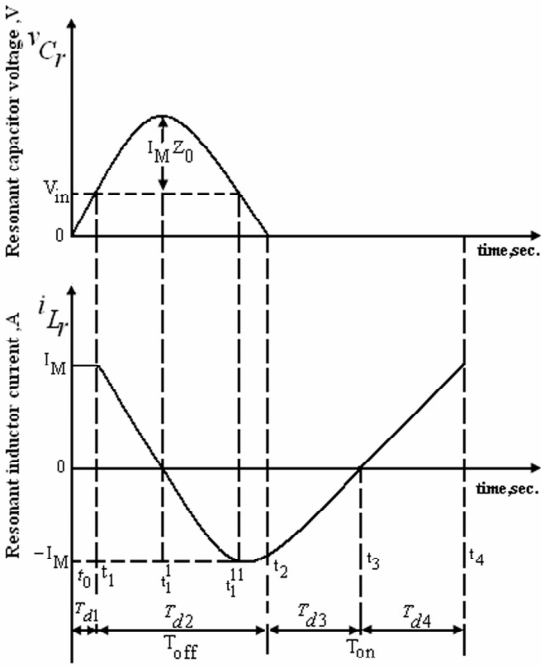


Fig. 3. Theoretical resonant waveforms of ZVS QR-NOSLL Converter

3. DC voltage conversion ratio of ZVS QR-NOSLL converter

In an ideal condition, from the conservation of energy theory, over a switching period, the input energy E_{in} is equal to the output energy E_0 and they can be described by the following equation:

$$E_{in} = V_{in}\left[\int_0^{T_{d1}/2} i_{L_r}(t)dt + \int_0^{T_{d4}} i_{L_r}(t)dt\right] \quad (13)$$

$$E_0 = V_0 I_0 T_S \quad (14)$$

Then the dc voltage conversion ratio is defined as

$$M = \frac{V_0}{V_{in}} = \frac{1}{T_S}\frac{I_M}{I_0}\left[T_S - \frac{T_{d1}}{2} - T_{d2} - T_{d3}\right] \quad (15)$$

By substituting the values of T_{d1} –T_{d3}, equation (15) is modified and expressed in terms of circuit parameter as

$$M = \frac{I_M}{I_0}\left[1 - \frac{I_0 C_r f_s R_0}{2MI_M} - \frac{\pi+\alpha}{2\pi}\times\frac{f_s}{f_0} + \frac{(I_M\cos\alpha)L_r f_s}{V_{in}}\right] \quad (16)$$

where

resonant frequency $f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$ (17)

normalized switching frequency $f_{ns} = \frac{f_s}{f_0}$ (18)

characteristic impedance $Z_0 = \sqrt{\frac{L_r}{C_r}}$ (19)

normalized load resistance $R = \frac{R_0}{Z_0}$ (20)

The non-linear equation (16) gives two solutions of M, out of which, the largest value is considered in the design. It is observed that, M is a function of R_0 and f_s. The value of M can be regulated by varying f_s.

4. Design of ZVS QR-NOSLL converter

The design parameters of the ZVS QR-NOSLL converter are calculated as follows:

The ZVS QR-NOSLL converter as shown in Fig. 1 is designed with the following parameters. V_{in}=12V, L_1= 10µH, C_1=C_2=10µF, I_0 = 2.4mA – 2A, V_0 = -24V.

The AC component of resonant voltage is

$$v_{C_r}(t) = Z_0 I_M \sin(\omega_0 t + \alpha) \quad (21)$$

where, the corresponding angular position α and I_M are given by

$$\alpha = \sin^{-1}\left(\frac{V_{in}}{Z_0 I_M}\right),\ I_M = (M_{\max}+1)I_0$$

and considering the DC component V_{in}, the peak voltage is

$$V_{C_{r-peak}} = V_{in} + Z_0 I_M \quad (22)$$

The condition for ZVS is given by

$$I_M Z_0 > V_{in} \quad (23)$$

To satisfy equation (23), choosing Z_0 = 7.4 Ω, normalised frequency f_{ns} = 0.4651 and resonant frequency f_0 = 215 KHz, the switching frequency (f_s) and resonant components (L_r and C_r) are calculated using equations (17) to (19) as 100 KHz, 5.5µH and 0.1µF respectively.

The ZVS QR-NOSLL converter is simulated using the general – purpose circuit analysis programme PSIM software with the designed parameters. The simulated waveforms of gate pulse, resonant capacitor voltage and resonant inductor current, are shown in Fig 4. It is observed from the results that, the switch S is turned ON, when the voltage across resonant capacitor becomes zero, thereby reducing switching losses. The simulated waveforms agree closely with the theoretical resonant waveforms shown in Fig. 3. The nominal output voltage and load current of the converter under open loop operation are shown in Figs.5 (a) and (b) respectively.

Voltage conversion ratio for different normalized switching frequency with different normalized load is given in table 1. The characteristics of voltage conversion ratio (M) versus normalized switching frequency (f_{ns}) for various normalized load R is shown in Fig. 6. At nominal operating condition R-13.5, the conversion ratio M is 1.85 for normalized switching frequency f_{ns} of 0.444. When R is suddenly changed from 13.5 to 6.76, M is decreased from 1.85 to 1.81. In order to maintain M at 1.85, the normalized switching frequency has to be varied from 0.444 to 0.44. Similarly when load is varied from 13.5 to 338, the M is increased from 1.85 to 1.99. In order to maintain M at 1.85, the normalized switching frequency has to be varied from 0.444 to 0.47. It is found that variation of M with f_{ns} is approximately linear and M is sensitive to the load R variations. Hence, a closed loop control is necessary to regulate the output voltage.

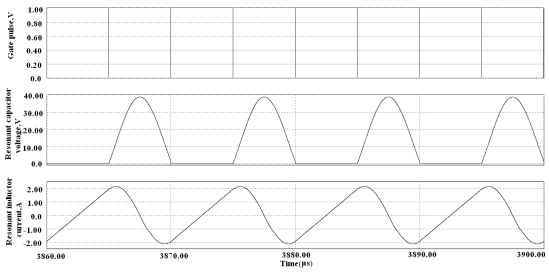
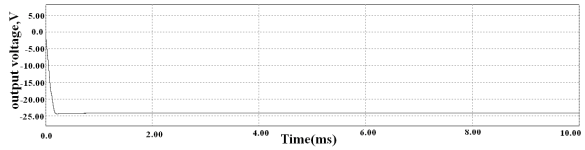
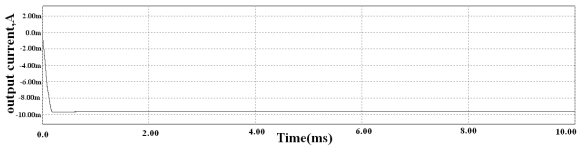


Fig. 4. Simulated resonant waveforms of ZVS QR NOSLL Converter



(a) Simulated output voltage of ZVS QR-NOSLL Converter



(b) Simulated load current of ZVS QR- NOSLL Converter

Fig. 5. Simulated output waveforms of ZVS QR- NOSLL Converter

Table 1. Voltage conversion ratio (M) for different normalized switching frequency (f_{ns}) with different normalized Load (R)

f_{ns} \ R	6.76	13.5	338
0.42	2.06	2.13	2.29
0.44	1.94	1.98	2.13
0.45	1.89	1.93	2.07
0.46	1.86	1.90	2.05
0.47	1.81	1.85	1.99
0.47	1.80	1.83	1.97
0.49	1.71	1.74	1.89
0.51	1.60	1.65	1.83

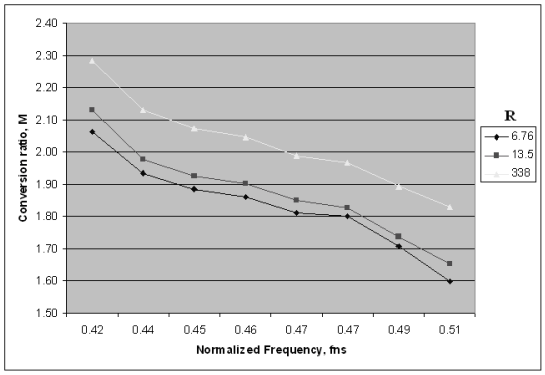


Fig. 6. Characteristics of normalized frequencies Vs Conversion ratio of ZVS QR-NOSLL Converter

5. Implementation of prototype ZVS QR-NOSLL converter

To verify the design outlined in the previous section ZVS NOSLL converter is implemented with the designed parameters. The photograph of the experimental setup is shown in Fig. 7. The inductors are made of ferrite core and the capacitors are of plain polyester. The diode FR306 is used as freewheeling diode as it is of fast recovery type and with high reliability. Power MOSFET IRF540 is used as active switch as it is dynamic and can carry high currents at high frequency with simple drive requirements. The experimental waveforms of resonant capacitor voltage with gate pulse , resonant inductor current with resonant capacitor voltage and load current with output voltage are shown in Figs.8 (a), (b), (c) respectively. It is observed that the switch S is turned on, when the resonant capacitor voltage becomes zero to ensure ZVS condition. This waveform resembles the simulated resonant waveforms as shown in Fig. 4. The discrepancy observed between the simulation and experimental waveforms may be due to parasitic components. Also the output voltage of the converter varies with change in load and supply. To provide output voltage regulation a closed loop control system is required.

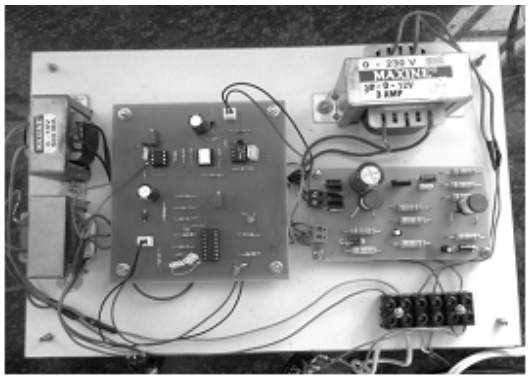
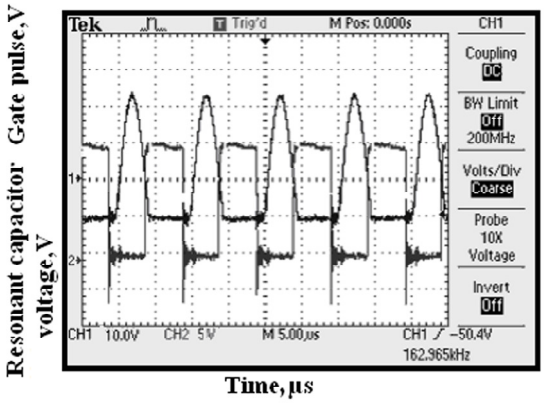
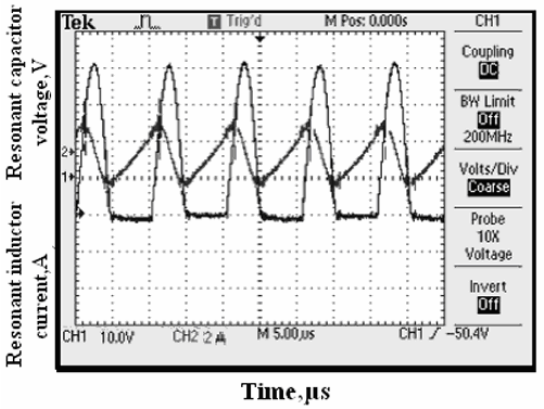


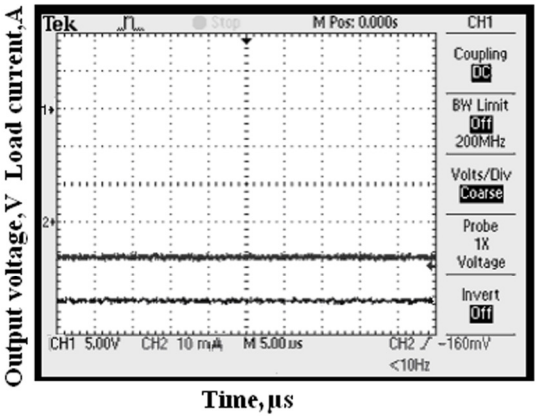
Fig. 7. Experimental implementation of ZVS QR-NOSLL converter



(a) Resonant Capacitor Voltage and Gate Pulse



(b) Resonant Inductor Current and Resonant capacitor voltage



(b) Output Voltage and Load Current

Fig. 8. Open loop experimental waveforms of ZVS QR-NOSLL Converter

5.1. Closed loop circuit of ZVS QR-NOSLL converter

The closed loop power circuit diagram of ZVS QR-NOSLL converter is shown in Fig.9. In the present work analog resonant controller UC3861 is used for voltage regulation. For closed loop operation, the output voltage is sensed and is directly fed through an 6N137 optocoupler to the non-inverting terminal of UC3861(Pin 2). The optocoupler is used to isolate the power circuit and control circuit. The power supply for the optocoupler is given from the 5V generator of UC3861 (Pin 1). This way no additional source is required, thereby reducing the size of the converter. Soft-Reference of the controller IC (Pin 16) is used as system reference, which is given to the inverting terminal of UC3861 (Pin 3). To achieve ZVS condition, the resonant capacitor voltage is given to the zero pin of UC3861 (Pin 10) through 6N137 optocoupler. The R_{RANGE} (Pin 6), R_{MIN} (Pin 7), and C_{Vco} (Pin 8) are selected to be 25KΩ, 200KΩ and 1nF so that the voltage-controller oscillator frequency varies between 21 KHz to 148 KHz which in turn determines the switching frequency of the pulses. The output of the oscillator serves as the internal clock and is given to trigger the one-shot timing generator. The one shot modulates the pulse width of gate signal depending on the zero crossing of $v_{C_r}(t)$.The output driver is directly connected to the gate of the MOSFET IRF540 through resister as shown in Fig. 9 Using the analog resonant controller, the switching frequency of gate pulse is varied to regulate the output voltage.

The performance of the closed loop system is studied for load and supply voltage disturbances. They are discussed as follows:
During closed loop operation the controller is able to keep the output equal to the set value of -24V for variation in supply of 3V (+ 25%) and the output voltage waveform is shown in Fig.10. The controller also acts effectively and gets back the output voltage to the reference value of -24V for 10% variations in load and the waveform is shown in Fig.11.The results show the merits of the analog resonant controller for the voltage regulation of ZVS QR-NOSLL converter.

The efficiency of the ZVS QR-NOSLL converter is calculated by obtaining the parasitic losses in the inductor, capacitors and conduction losses of switching devices. The losses are calculated experimentally by measuring the rms value of the currents in the above-mentioned components. The maximum efficiency at full load is found to be 96%. Therefore, the proposed ZVS QR-NOSLL converter has low switching losses, high voltage transfer gain, high reliability and less electromagnetic interference and acoustic noise compared to existing conventional pulse width modulated NOSLL converter.

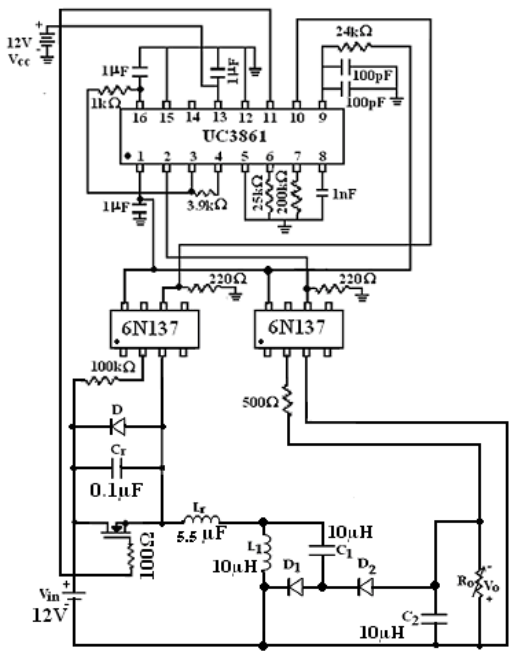


Fig. 9. Power circuit for closed-loop control

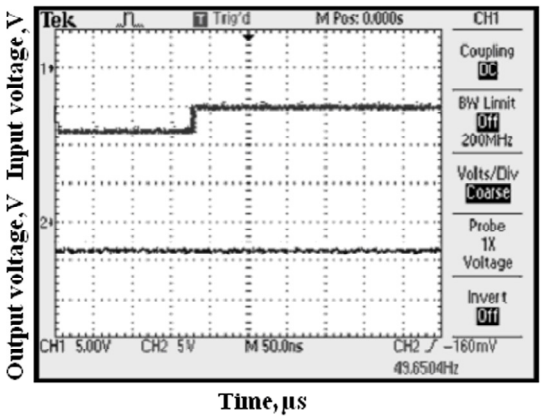


Fig.10. Regulated output voltage for increase in Input voltage [Ch1 (5V/div) and Ch2 (5V/div) wave forms denotes Output Voltage and Input voltage]

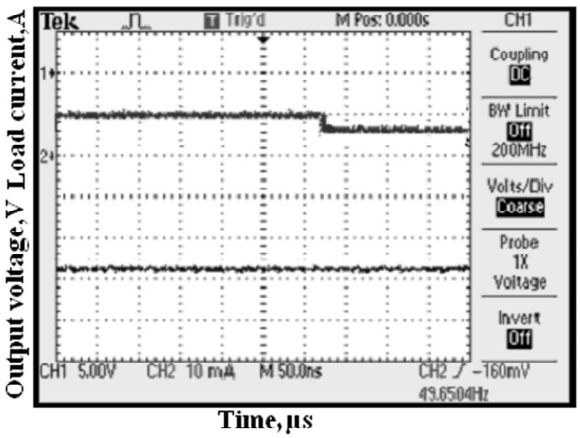


Fig.11. Regulated output voltage for decrease in load current [Ch1 (5V/div) and Ch2 (10mA/div) waveforms denotes Output voltage and load current]

6. Conclusion

In this paper, a method of voltage control for ZVS QR-NOSLL converter using a simple dedicated IC UC3861 is proposed. The theoretical waveforms agree with the simulated results. Also during closed loop operation better voltage regulation is obtained for load variations and supply disturbances. The complexity in designing analog pulse generating circuit, additional power supply requirement and sophisticated protection circuit are not required in the proposed control method and hence the size of the converter is reduced. This method of control is suited for any application requiring constant power supply and is mainly designed for power supply in aerospace applications.

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