COMBINED METHOD USING NVM AND SHC FOR SPACE FPGAs

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Abstract:

In space application, the devices are required to retain data even when there is no power available. For that nonvolatile Memory, flash memories are used. But they have the limitation of onetime programming capability. Recently all FPGAs in space utilizes multi time programming SRAM technology but introducing soft errors in data and parity of these memories is the major issue for long-term retention. In this paper, to remit, the soft errors non-volatile SRAM Memory is proposed, and for encoding encode-and-compare scheme is built with 2-D Symbolic Hamming Matrix Code. To reduce leakage power, a low power memory cell has been used which uses positive ground voltage. The proposed method requires a short time for detecting the error and it has the capability to detect and correct a more number of soft errors.

Keywords: *NVSRAM, Symbolic Hamming Matrix Code, Reliability*
Classification: *Circuits and modules for storage*

1. INTRODUCTION

In Space applications, the nonvolatile memories are used to store data or code for future missions. Ionizing radiations damage the space-related applications that may create a bit flip in memory. Static Random-Access Memory (SRAM) based Field Programmable Gate Array (FPGA) is vulnerable to ionizing radiation resulting in radiation-induced memory upset. For solving radiation effects Resistive Random-Access Memory (RRAM) based FPGA is chosen. Nonvolatile memory is the devices that hold data even when there is no power supply. Non-volatile memories are consumed some time to read and write the data in it but it can recover the data without power supply. It is a most common method for long-term retention. SRAM can perform read and write but non-volatile SRAM perform read, write, store and recall. Soft errors are one of the problems to considering memory. Soft error changes the instruction in program or data value. To mitigating the soft error (SE) many techniques are preferred. One such technique to mitigate the soft error is Error Correction Codes (ECC). ECC requires storage of information for error detection [4]. It stores enough information for error detection and detection by means of extra bits. This improves the system reliability [5]. RRAM has extremely high tolerance to soft error upsets and multiple bits upset. Error correction is chosen for data integrity.

2. Existing Mitigation Techniques

In the traditional error correction method, encoded data was applied to the SRAM memory or Flash for storing the data and parity is shown in Fig 1. When using SRAM it increases the internal speed. High speed could increase the soft error rates because memory cells are vulnerable to an error during read, write operations [1]. These soft errors affect the performance of the device. Soft errors are solved by resetting and restore normal behavior of data but it is impossible for all devices. Flash memory is the electronic non-volatile storage device. One limitation of flash memory is, it can be read a word at only one time.

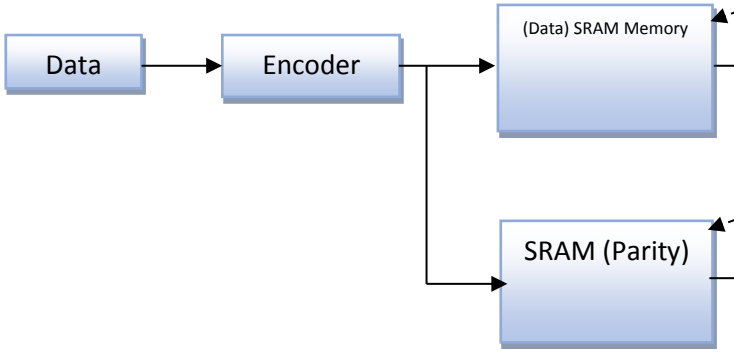

Fig 1: Traditional soft error mitigation Technique

3 Proposed mitigation Technique

To overcome the limitation of existing method Non-Volatile SRAM (NVSRAM) is proposed for storing the parity data as well as to improving the reliability of data. The proposed block diagram is shown in Fig 2.

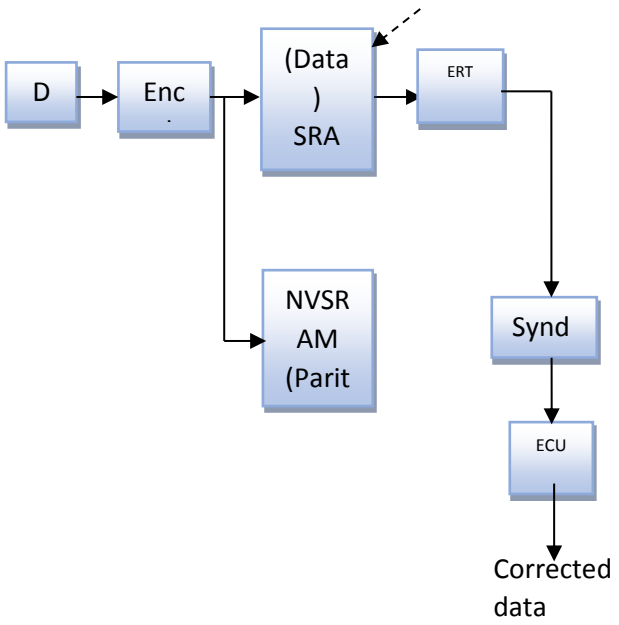

Fig 2: Proposed soft error mitigation Technique

3.1. NVSRAM Design

NVSRAM designed to shrink the leakage power of the cell and maintain the data stored during the idle state. The NVSRAM cell suggested in [2-3] required enormous amount of charge, so it is particularly tolerant to Single Error Upset (SEU). Also, this implicit an NVSRAM cell stored the parity in the non-volatile element. The improved design of 13T1R NVSRAM cell is shown in Fig 3. For better SEU tolerance and other performance metrics (write/read), the volatile hardened cells use a positive virtual ground technique [4-6]. Table I shows the values of the different parameters used in memory. Table II shows the values of the performance of NVSRAM at 32nm technology. RRAM are two node electronic devices with three layered architecture i.e. metal oxide embedded within the top and bottom electrode. [7] [8].

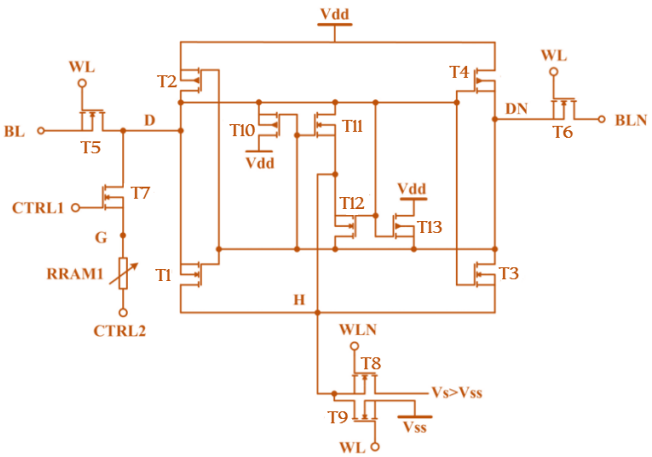

Fig 3: Proposed 13T1R NVSRAM cell for storing Parity bit

Table I. Parameters for memory cell simulation

Parameter	Value
Temperature	25 C
Feature size	32 nm
Vdd	0.9 V
CTRL1, CTRL2	0.9 V

Table II. Performance of 13T1R NVSRAM at 32 nm

Vs	Write Time (ps)	Read Time (ps)	Storage Node Charge (fC)
0 V	32.32 ps	39.45 ps	2.345 fC
0.1 V	32.41 ps	39.52 ps	1.844 fC
0.2 V	32.46 ps	39.61 ps	1.371 fC

3.2. 2-D Symbol wise Hamming Code

The configuration words are arranged in the form of a matrix with divide by symbol. This process is known as fine grain mechanism. This mechanism upgrades the reliability and operation speed. N-bit word is divided into K symbols and m bits/symbol. The value of K calculated by K= A×B where A and B represent a number of rows and columns respectively.

Fig 4: 2-D SHC redundant bits calculation

In 2-D SHMC 32 bit configuration word is considered. In this 32-bit, 24 number of redundant bits are determined to alter the errors. In each symbol, parity redundant bits are generated by using SECDED (7,4) calculation. For example in fig 4, redundant bits are calculated by using equations (1) - (3). Likewise, the redundant bits for all symbols are generating. Encode compare mechanism is used to reduce

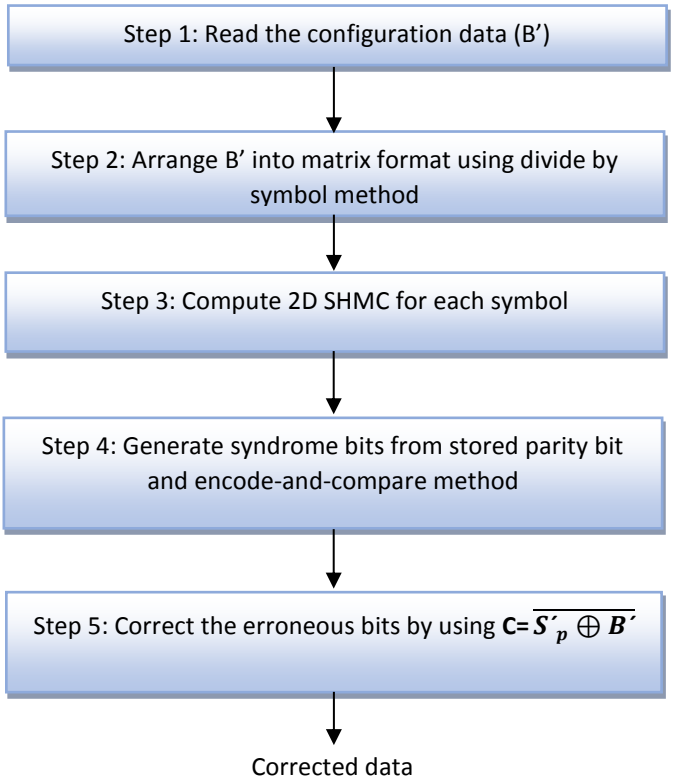

Fig 5: Flowchart for 2-D SHC method

$$B_0 \oplus B_1 \oplus B_3 = H_0 \quad (1)$$

$$B_0 \oplus B_2 \oplus B_3 = H_1 \quad (2)$$

$$B_1 \oplus B_2 \oplus B_3 = H_2 \quad (3)$$

At last difference between stored and recalculated redundant bits computing or finding the syndrome value (Sp´). Finally step.5 correct the softerror.

4.Result and Discussion

The experimentation of the proposed work is done in Tanner EDA software and the simulation is done in Xilinx for FPGA analysis. Fig. 6 shows the power dissipation for different types of memory with Vs= 0.1 V and different feature sizes. Three types of NVSRAM and 6T SRAM are estimated and compared based on some specific operations. Proposed NVSRAM has no power dissipation compared with 6T SRAM. 13T1R NVSRAM has lower power dissipation than 9T1R NVSRAM since the internal nodes are linked to the virtual ground.

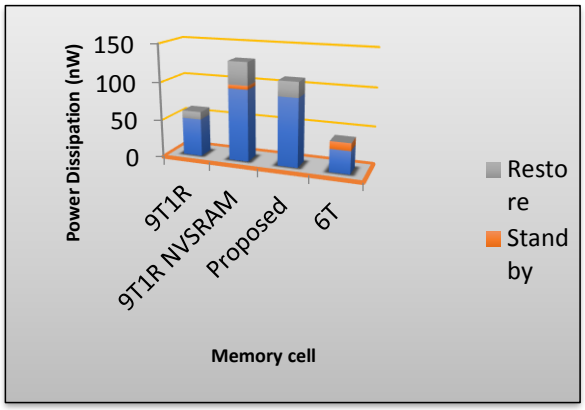

Fig. 6. Power Dissipation comparison

Fig. 7 shows the Performance of Read/Write operation of the same four memory cells. Performance of Read/Write operation for the proposed method is better than the other methods read/write operation. During Write operation, WL= 1 and the T9 transistor will be turned ON. In Transistor T9 charge and discharge capacitance increase by adding drain-source capacitance value.

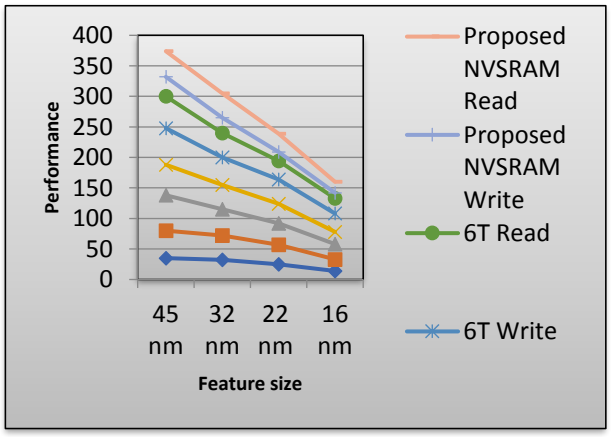

Fig. 7. Performance Vs Different memory cell

Soft Error Rate (SER) is a crucial parameter for robustness to soft errors. The soft errors are depending on characteristics of the device. In SER specific portion of each component depends on specific conditions. Fig. 8 shows the average Single Error Rate versus feature size.

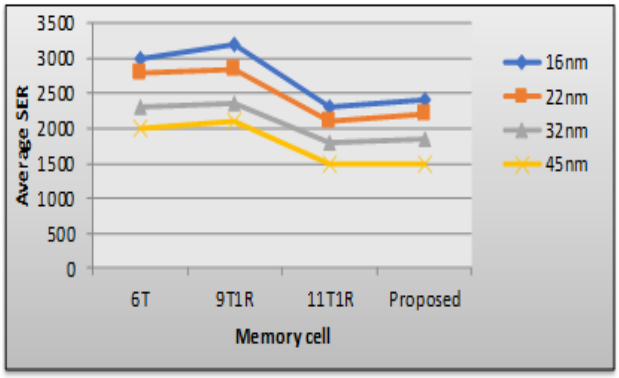

Fig 8: Memory cell Vs Average SER

5. CONCLUSION

In this paper, Non-volatile Static Random-Access Memory is proposed for solving the soft error occurring in the memory cells. These memory cells are performing their operation by using a single resistive element. These single resistive elements produce the soft errors in the Memory. The proposed non-volatile SRAM store the code without introducing errors in parity. In addition to reducing delay time, an encode-and-compare scheme with 2-D SHC is provided. This scheme requires a short time for detecting the error and it has the capability to detect and correct a large number of errors.

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